Usage of the DBBC3 firmware and software

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Sven Dornbusch, MPIfR

Max-Planck-Institut
für Radioastronomie

MAX-PLANCK-GESELLSCHAFT

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Observation Modes

Observation Modes

- DSC
- OCT
- DDC

Observation Modes

- **DSC**
- OCT
- DDC

- Direct Sampling Conversion
- 4GHz Bandwidth/IF
- Produces four 4Gbit/s streams per IF
- Recombination of recorded streams required

Observation Modes

- DSC
- **OCT**
- DDC

- (OCT)opus Mode
- 2 parallel FIR-Filters/IF
- Bandwidth of 256/512/1024/2048 MHz for each Filter
- Produces two output streams with up to 8Gbit/s each

Observation Modes

- DSC
- OCT
- **DDC**

- DDC_V: (VGOS)
  - 8 tunable BBCs/IF with upper/lower sideband each
  - 32 MHz BW/sideband
  - Specialized filters for 32MHz
- DDC_U (Universal)
  - 16 tunable BBCs/IF with upper/lower sideband each
  - 2, 4, 8, 16, 32, 62, 128 MHz BW/sideband
- DDC_E (EVN)
  - 8 tunable BBCs/IF with upper/lower sideband each
  - 2, 4, 8, 16, 32, 62, 128 MHz BW/sideband
  - Improved filters

Preparations

# Hardware Connections

- Necessary Connections on the Back:
  - 10 MHz
  - 1 PPS
  - GPS
  - Signal Input 0-4 GHz
  - Or Signal Input 4-15 GHz
    - with Down conversion
    - Connect "Out (unfilt.)" to "0-4 GHz in"
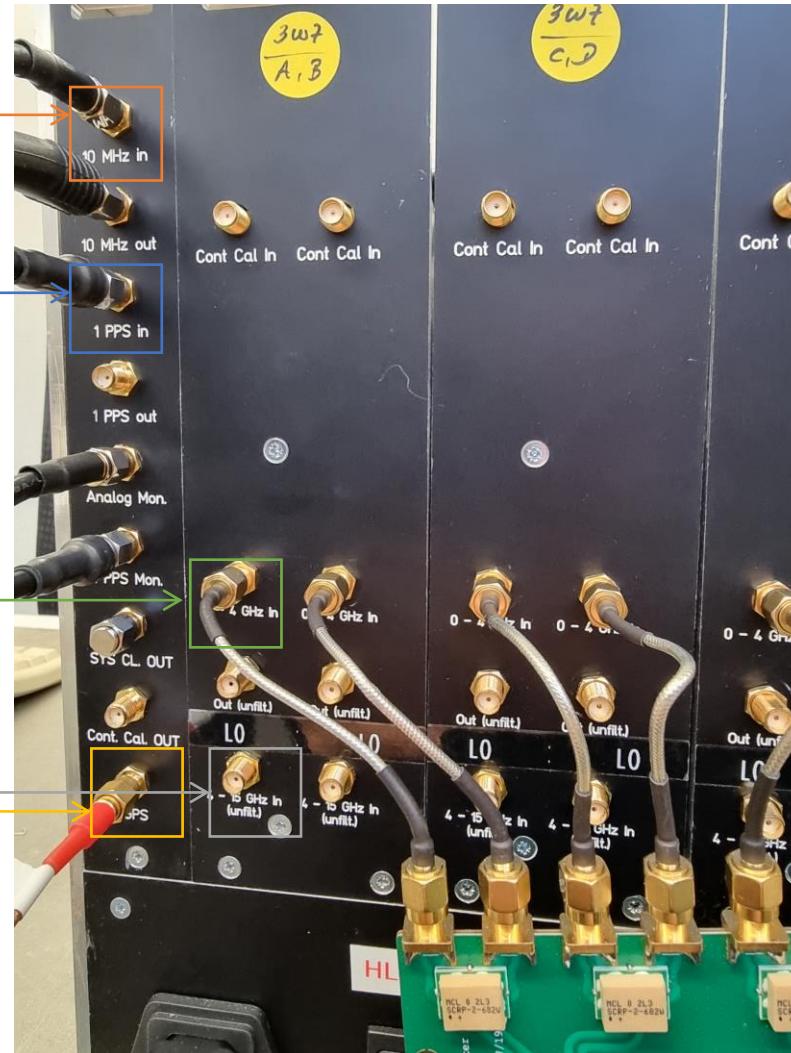
Hardware Connections

- Ethernet Output:
  - 4 Ethernet Ports/IF
  - DDC_V/E: Port 0
  - DDC_U: Port 0 and 1
    - BBCs 1-8: Port 0
    - BBCs 9-16: Port 1
  - OCT: Port 0 and 2
    - Filter 1 Port 0
    - Filter 2 Port 2
  - DSC: Port 0-3
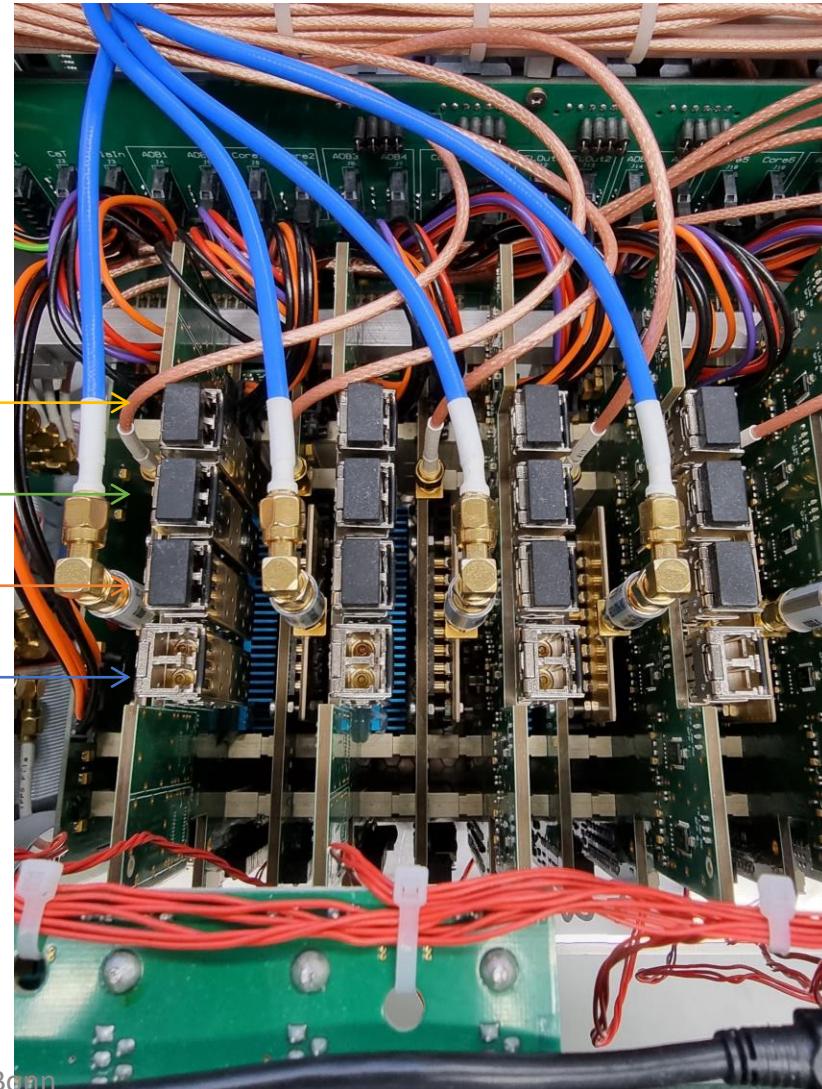
Software Components

- Control Software
- Client
- Firmware
- Configuration Files
- Python Toolkit
- Field System

Software Components

- **Control Software**

- Client

- Firmware

- Configuration Files

- Python Toolkit

- Field System

- Located in C:\DBBC\bin folder

- One exe-File for each Observation Mode:
  - DBBC3 Control DSC_v120.exe
  - DBBC3 Control OCT_D_v120.exe
  - DBBC3 Control DDC_V_v125.exe
  - DBBC3 Control DDC_E_v126.exe
  - DBBC3 Control DDC_U_v126.exe

- Link to each File on Desktop

Software Components

- Control Software
- **Client**
- Firmware
- Configuration Files
- Python Toolkit
- Field System

- Located in C:\DBBC\bin folder
- DBBC client v4.exe
- Local Client used to communicate with Control Software
- Link on Desktop

Software Components

- Control Software
- Client
- **Firmware**
- Configuration Files
- Python Toolkit
- Field System

- Located in C:\DBBC_CONF\FilesDBBC folder
- One bit-File for each Observation Mode:
  - dbbc3_dsc_2hv2_070922.bit
  - dbbc3_oct_D_2hv2_310822.bit
  - dbbc3_ddc-v125V-2hv2-120922.bit
  - dbbc3_ddc-v126E-2hv2_231022.bit
  - dbbc3_ddc_U_v126-2hv2_271122_2.bit

Software Components

- Control Software

- Client

- Firmware

- **Configuration Files**

- Python Toolkit

- Field System

- Located in C:\DBBC_CONF folder
  - C:\DBBC_CONF\DSC_120 for DSC Mode
  - C:\DBBC_CONF\OCT_D_120 for OCT_D Mode
  - C:\DBBC_CONF for all DDC Modes

- Five types of configuration files
  - Main config file
  - Sampler config file
  - Core3H config files (one for each IF)
  - BBC config file (for DDC modes)
  - Filter tap files (for OCT_D mode)

Main Config File

- Example: dbbc3_config_file_ddc_E_126.txt

- References to other config files

- Init Part for Core3H-Boards

- Init Part for GCoMo-Modules

- Synthesizer Config

- IP-Address of DBBC3

- IP and Port for Multicast Group

- Maximum Number of Phasechecks

```
config_adb3l.txt
config_ddc_E.txt
```

```
3 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_1.fila10g COM3
3 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_2.fila10g COM4
30 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_3.fila10g COM5
30 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_4.fila10g COM6
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_5.fila10g COM7
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_6.fila10g COM8
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_7.fila10g COM9
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_8.fila10g COM10
```

```
3 4500 10 32000 COM11
3 4500 10 32000
3 4500 10 32000 COM12
3 4500 10 32000
0 28000
0 28000
0 28000
0 28000
```

```
CAT3 2048
```

```
134.104.30.223
```

```
224.0.0.255:25000
```

```
20
```

Main Config File

- Init Part for Core3H-Boards
  - Core3H Status:
    - 3: Installed Core3H and Signal connected to IF
    - 30: Installed Core3H and NO Signal connected
    - 0: No Installed Core3H
  - Core3H Firmware
  - Core3H Config File
  - Serial COM Port

```
config_adb3l.txt
config_ddc_E.txt
3 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_1.fila10g COM3
3 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_2.fila10g COM4
30 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_3.fila10g COM5
30 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_4.fila10g COM6
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_5.fila10g COM7
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_6.fila10g COM8
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_7.fila10g COM9
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_8.fila10g COM10
3 4500 10 32000 COM11
3 4500 10 32000
3 4500 10 32000 COM12
3 4500 10 32000
0 28000
0 28000
0 28000
0 28000
CAT3 2048
134.104.30.223
224.0.0.255:25000
20
```

Main Config File

- Init Part for GCoMo-Modules
  - GCoMo Status:
    - 3: Installed
    - 0: Not Installed
  - Synthesizer Frequency for Down Conversion
    - In MHz
    - ½ of LO-Frequency
  - Attenuation for Synthesizer Frequency
    - in dBm
  - AGC Power Target
  - COM Port for Synthesizer Communication
    - 2 IFs share one Synthesizer (with 2 Outputs each)

```
config_adb3l.txt
config_ddc_E.txt
3 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_1.fila10g COM3
3 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_2.fila10g COM4
30 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_3.fila10g COM5
30 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_4.fila10g COM6
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_5.fila10g COM7
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_6.fila10g COM8
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_7.fila10g COM9
0 dbbc3_ddc-v126E-2hv2_231022.bit ddc_E_core3H_8.fila10g COM10
3 4500 10 32000 COM11
3 4500 10 32000
3 4500 10 32000 COM12
3 4500 10 32000
0 28000
0 28000
0 28000
0 28000
CAT3 2048
134.104.30.223
224.0.0.255:25000
20
```

Sampler Config File

- Example: adb3l_config.txt
  - Static Part
    - Do not Change
  - Delay, offset and gain for each sampler
    - command=board,sampler,value
    - board[1-8]
    - sampler[0-3]
    - Value determined by Calibration Procedure
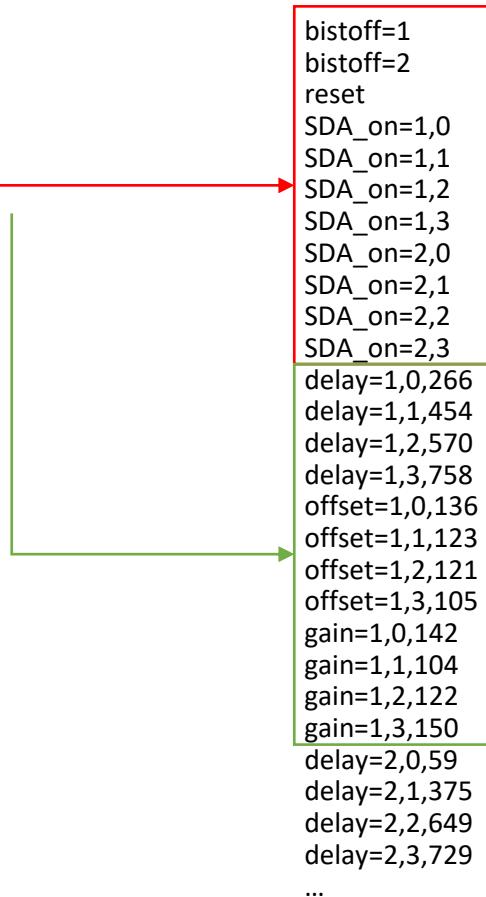
```
bistoff=1
bistoff=2
reset
SDA_on=1,0
SDA_on=1,1
SDA_on=1,2
SDA_on=1,3
SDA_on=2,0
SDA_on=2,1
SDA_on=2,2
SDA_on=2,3
delay=1,0,266
delay=1,1,454
delay=1,2,570
delay=1,3,758
offset=1,0,136
offset=1,1,123
offset=1,2,121
offset=1,3,105
gain=1,0,142
gain=1,1,104
gain=1,2,122
gain=1,3,150
delay=2,0,59
delay=2,1,375
delay=2,2,649
delay=2,3,729
…
```

Core3H Config Files

- Example: ddc_U_core3H_1.fila10g
  - Static Parts, do not Change

```
core3_init
core3_mode pfb
regwrite core3 0 0x00000000
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1-2-3-4
vsi_samplerate 128000000
splitmode on
reset
vdif_frame 2 16 8000 ct=off
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:42:38:e2
destination 0 192.168.1.2:46220
destination 1 none
timesync
start vdif
sysstat
```

Core3H Config Files

- Example: ddc_U_core3H_1.fila10g

  - vsi_samplerate:
    - DDC_U/E: Change according to used BBC-bandwidth:
      - 128 MHz: vsi_samplerate 128000000
      - 64 MHz: vsi_samplerate 128000000 2
      - 32 MHz: vsi_samplerate 128000000 4
      - 16 MHz: vsi_samplerate 128000000 8
      - 8 MHz: vsi_samplerate 128000000 16
      - 4 MHz: vsi_samplerate 128000000 32
      - 2 MHz: vsi_samplerate 128000000 64
    - DDC_V: keep at vsi_samplerate 128000000 2
    - DSC/OCT_D: command not used

```
core3_init
core3_mode pfb
regwrite core3 0 0x00000000
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1-2-3-4
vsi_samplerate 128000000
splitmode on
reset
vdif_frame 2 16 8000 ct=off
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:42:38:e2
destination 0 192.168.1.2:46220
destination 1 none
timesync
start vdif
sysstat
```

Core3H Config Files

- Example: ddc_U_core3H_1.fila10g

  - vdif_frame:

    - Bits/sample: default 2

    - #Channels/vdif_frame: default 2x(#BBCs/Output Port)
      change if using vsi_bitmask to mask out channels!
      Not #Channels in total, be careful with DDC_U!

    - Data-Bytes/Frame: default 8000

    - ct=off, do not change, Corner Turning not implemented on
      DBBC3

```
core3_init
core3_mode pfb
regwrite core3 0 0x00000000
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1-2-3-4
vsi_samplerate 128000000
splitmode on
reset
vdif_frame 2 16 8000 ct=off
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:42:38:e2
destination 0 192.168.1.2:46220
destination 1 none
timesync
start vdif
sysstat
```

Core3H Config Files

- Example: ddc_U_core3H_1.fila10g

    - Configuration of Ethernet Ports

        - tengbcfg: set source configuration for ethernet port

        - tengbarp: set the destination MAC-addresses for ethernet port and subnet

        - destination: set destination IP and Port for given output stream
        set to none if output is not used

```
core3_init
core3_mode pfb
regwrite core3 0 0x00000000
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1-2-3-4
vsi_samplerate 128000000
splitmode on
reset
vdif_frame 2 16 8000 ct=off
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:42:38:e2
destination 0 192.168.1.2:46220
destination 1 none
timesync
start vdif
sysstat
```

Core3H Config Files – Bitmask

- vsi_bitmask to mask out channels:

- Take special care with DDC_U!:
  - vsi_bitmask mask2 mask1 mask2 mask1
    mask1 = Bitmask for BBCs 1-8
    mask2 = Bitmask for BBCs 9-16

- DDC_E:
  - vsi_bitmask mask1 mask1 mask1 mask1

- All 4 masks need to have the same number of bits

- If you mask out channels, always adjust the number of channels in the vdif_frame accordingly!

- More Info about setting the bitmask:
  https://deki.mpifr-bonn.mpg.de/Cooperations/DBBC3/DBBC3_FAQ?highlight=FAQ

```
core3_init
core3_mode pfb
regwrite core3 0 0x00000000
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1-2-3-4
vsi_samplerate 128000000
splitmode on
vsi_bitmask 0x33333333 0x33333333 0x33333333 0x33333333
reset
vdif_frame 2 16 8000 ct=off
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:42:38:e2
destination 0 192.168.1.2:46220
destination 1 none
timesync
start vdif
sysstat
```

Core3H Config Files – Change Thread ID

- To Change the Base Thread ID:
  - Calculate value: $V = thread\_Id * 2^{16}$
  - regupdate vdif_header 3 V 0x03FF0000
  - This is the base thread ID for Port eth0
  - eth1 will have base thread ID + 1, and so on…

```
core3_init
core3_mode pfb
regwrite core3 0 0x00000000
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1-2-3-4
vsi_samplerate 128000000
splitmode on
reset
vdif_frame 2 16 8000 ct=off
regupdate vdif_header 3 327680 0x03FF0000
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:42:38:e2
destination 0 192.168.1.2:46220
destination 1 none
timesync
start vdif
sysstat
```

BBC Config File

- Initial Configuration for the BBCs:
  - BBC Number (1-128)
  - Frequency
  - Bandwidth

- BBC Numbering for DDC_U:

Board 1	Board 2	Board 3	Board 4	Board 5	Board 6	Board 7	Board 8
1-8	9-16	17-24	25-32	33-40	41-48	49-56	57-64
65-72	73-80	81-88	89-96	97-104	105-112	113-120	121-128

```
1 300.0 128
2 300.0 128
3 300.0 128
4 300.0 128
5 300.0 128
6 300.0 128
7 300.0 128
8 300.0 128
9 300.0 128
10 300.0 128
11 300.0 128
12 300.0 128
13 300.0 128
14 300.0 128
15 300.0 128
16 300.0 128
10 300.0 128
11 300.0 128
12 300.0 128
13 300.0 128
14 300.0 128
15 300.0 128
16 300.0 128
…
```

Startup Routine

Startup Routine

1. Start Control Software on Desktop

2. Load Firmware(Y/N)
   (Can be skipped if correct firmware already loaded)

3. Load Configuration(Y/N)

4. Connect with Client/Python Tool/FS

5. Perform Post-Startup System Checks

6. Ready for Observation
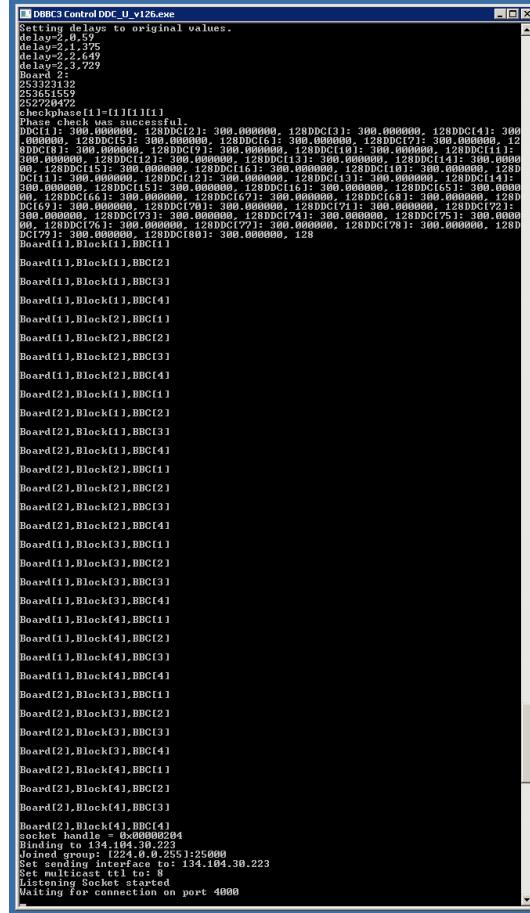
Post-Startup System Check

Post-Startup System Check

1. Check GCoMo Power Levels

2. Phasecheck

3. Check PPS Synchronization

4. Check Time Synchronization

5. Check Sampler Statistics

6. Check BBC Statistics

Post-Startup System Check

1. **Check GCoMo Power Levels**

2. Phasecheck

3. Check PPS Synchronization

4. Check Time Synchronization

5. Check Sampler Statistics

6. Check BBC Statistics

- Use **dbbcifa**, **dbbcifb**, … commands to check if each used GCoMo has the correct power levels:

- dbbcifa/2,**20**,agc,**31433**,32000
  - GCoMo Input (1-Direct Input, 2-Down Conversion)
  - Attenuation level (ideally between 10-40)
  - Automatic Gain Control (agc – AGC on, man – AGC off)
  - Power Level (should close to power target)
  - Power Target (32000 ideal for 4 GHz Input)

Post-Startup System Check

1. Check GCoMo Power Levels

2. **Phasecheck**

3. Check PPS Synchronization

4. Check Time Synchronization

5. Check Sampler Statistics

6. Check BBC Statistics

- **Command: checkphase**
  - This command will check if phases for the used samplers are correctly aligned
  - If the check fails, make sure that the **GCoMo Power Levels** for the failed Board are correct, and repeat the check.
  - If the check still fails, **restart the Control Software**. Loading the Firmware can be skipped.
  - If the check still fails, there may be a **hardware issue**. Contact Support. Include the latest logfile (in Folder C:\)

Post-Startup System Check

1. Check GCoMo Power Levels

2. Phasecheck

3. **Check PPS Synchronization**

4. Check Time Synchronization

5. Check Sampler Statistics

6. Check BBC Statistics

- **Command: pps_delay**
  - Checks the delay between internal (generated) and external PPS
  - Should be **below 100ns** for each used IF.
  - **Restart Control Software** if Value too high. Loading Firmware can be skipped.
  - **Careful**: If the external PPS comes from the GPS, there may be a drift between internal and external PPS over time.

Post-Startup System Check

1. Check GCoMo Power Levels

2. Phasecheck

3. Check PPS Synchronization

4. **Check Time Synchronization**

5. Check Sampler Statistics

6. Check BBC Statistics

- **Command: core3h=board_nr, time**
  - board_nr from 1-8
  - Check that the **timestamp** is correct.
    1-2 sec off is ok due to serial communication delay.
  - If not, **check GPS connection** and **restart Control Software**.
    Loading Firmware can be skipped.

Post-Startup System Check

1. Check GCoMo Power Levels

2. Phasecheck

3. Check PPS Synchronization

4. Check Time Synchronization

5. **Check Sampler Statistics**

6. Check BBC Statistics

- **Command: core3hstats=board_nr**
  - "**Core3H[] Power**" The four values should be less than 1-2% off from each other.
    If not, a recalibration of the **gain** might be required.
  - Example:
    Core3H[1] Power:
    Sampler 0: 62547223
    Sampler 1: 62732176
    Sampler 2: 62415746
    Sampler 3: 61841107
  - "**Core3H[] Bstat**." 50%/50% distribution between first two and last two values for each sampler.
    If not, a recalibration of the **offset** might be required.
  - Example:
    Sampler 0:
    11:      54 0.35%
    10:    7763 49.68%
    01:    7767 49.71%
    00:      38 0.24%

Post-Startup System Check

1. Check GCoMo Power Levels

2. Phasecheck

3. Check PPS Synchronization

4. Check Time Synchronization

5. Check Sampler Statistics

6. **Check BBC Statistics**

- **Command: dbbcXX**
  - Replace XX with the BBCs number (01-128)
  - Example response:
    dbbc001/ 300.000000,a,128,1,agc,26,26,15244,15004,0,0;
  - Check that **frequency** and **bandwidth** are correct
  - Power levels should be around 15k,
    gain within range (0-255), but this is a recommendation,
    not a strict requirement

Calibration

Calibration

- When do you need to recalibrate?
  - **Gain**: Core3H-Power is systematically off during Post-Startup System Check
  - **Offset**: Core3H-Bstat is systematically off during Post-Startup System Check
  - **Delay**: Always recalibrate if you needed to recalibrate gain or offset.
  - Check for **RFI** in the band first, this can in some cases lead to deviation in gain and offset.

- **Only perform calibration if you have a clean 4GHz Signal source**:
  - 4 GHz bandwidth clean noise (from noise generator or receiver)
  - Power must be stable during the calibration process!!!
  - Enough Power (32k GCoMo Power Level)
  - No RFI in the band!!!

Offset-Calibration

1. **Increase the attenuation** of the corresponding GCoMo so that the **power level is between 5 and 10k**:
    - dbbcifa=2,40
    - dbbcifa/ 2,40,man,1,**5557**,32000;

2. Issue the Command: **cal_offset=board_nr[1-8]**
    - Example: cal_offset=1
    - The result is shown in the Command windows of the Control Software, not the Client:
      Sampler[0], best offset 136
      offset=1,0,136
      Sampler[1], best offset 124
      offset=1,1,124
      Sampler[2], best offset 120
      offset=1,2,120
      Sampler[3], best offset 102
      offset=1,3,102

3. Change the values in the **config_adb3l.txt** according to the result of the calibration
    - offset=1,0,136
      offset=1,1,124
      offset=1,2,120
      offset=1,3,102

4. **Reset the attenuation** in the GCoMo to agc to reach power level of 32k, restarting the control software is not necessary
    - dbbcifa=2,agc

Gain-Calibration

1. Make sure the power level of the GCoMo is **around 32k**, **manual mode** is recommended:
   - dbbcifa=2,man
   - dbbcifa/ 2,4,man,1,**32443**,32000;

2. Issue the Command: **cal_gain=board_nr[1-8]**
   - Example: cal_gain=1
   - The result is shown in the Command windows of the Control Software, not the Client:
     Sampler[0], best gain 129
     Sampler[1], best gain 97
     Sampler[2], best gain 128
     Sampler[3], best gain 159

3. Change the values in the **config_adb3l.txt** according to the result of the calibration
   - gain=1,0,129
     gain=1,1,97
     gain=1,2,128
     gain=1,3,159

4. **Reset the attenuation** in the GCoMo to agc, restarting the control software is not necessary.
   - dbbcifa=2,agc

Delay-Calibration

1. Make sure the power level of the GCoMo is **around 32k**, **manual mode** is recommended:
   - dbbcifa=2,man
   - dbbcifa/ 2,4,man,1,**32443**,32000;

2. Issue the Command: **cal_delay=board_nr[1-8]**
   - Example: cal_delay=1
   - The result is shown in the Command windows of the Control Software, not the Client
     0->1, Best difference = 194 with corr_value = 244646768
     1->2, Best difference = 142 with corr_value = 244000252
     2->3, Best difference = 214 with corr_value = 243237046
     Sampler[0]->delay=247
     delay=1,0,247
     Sampler[1]->delay=441
     delay=1,1,441
     Sampler[2]->delay=583
     delay=1,2,583
     Sampler[3]->delay=797
     delay=1,3,797

3. Change the values in the **config_adb3l.txt** according to the result of the calibration
   - delay=1,0,247
     delay=1,1,441
     delay=1.2.583
     delay=1.3.797

4. **Reset the attenuation** in the GCoMo to agc, restarting the control software is not necessary.
   - dbbcifa=2,agc

Thank you, any questions?