BRAND STATUS UPDATE

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On behalf of the BRAND team:

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BRAND PROJECT

- BRAND was part of EC-funded Joint Research Activity (JRA)
- Formally ended end of 2020
- Goal: build broad band receiver prototype for Effelsberg
  - 1.5 -15.5 GHz
  - Direct sampling; no down-conversion

- Status:
  - Finished: analogue components, feed, digital backend
  - Delayed: finalization of digital frontend
  - Pending: construction of shielding box (depends on digital frontend)

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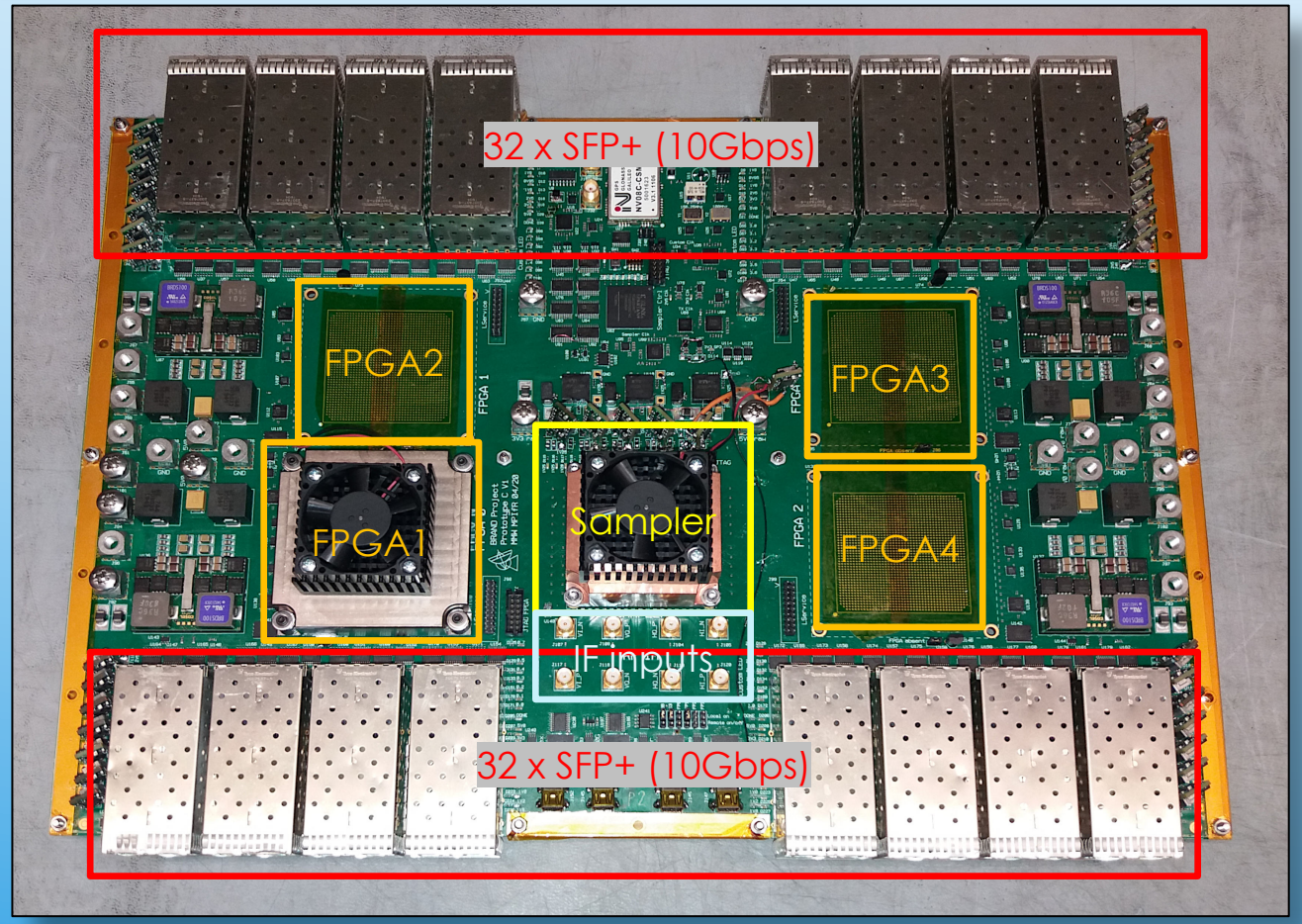
BRAND DIGITAL FRONTEND



BRAND_C (PCB 3rd revision)
- 30x40 cm
- 22 layers

IF Inputs (2 options):
- 2 x 28 GHz
- 4 x 14 GHz

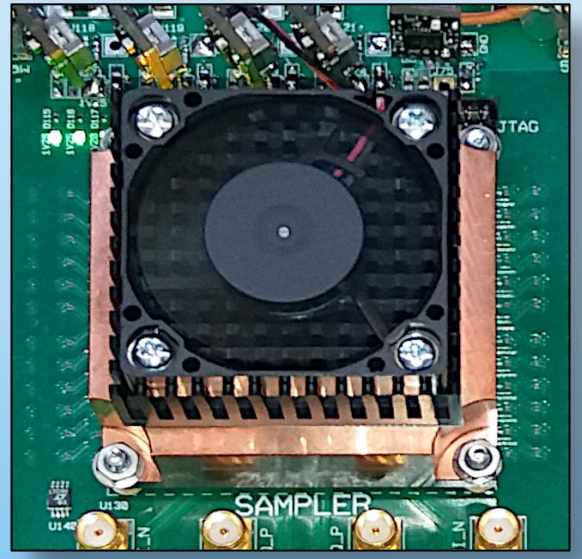
Outputs:
- 64 x 10 Gbit

FPGAs:
- 4 x Xilinx Kintex Ultrascale

Sampler:
- 112 Gsps @8bit

Power supply
- Max. 100A @ 0.95V (FPGA)

BRAND DIGITAL FRONTEND - SAMPLER



Sampler:

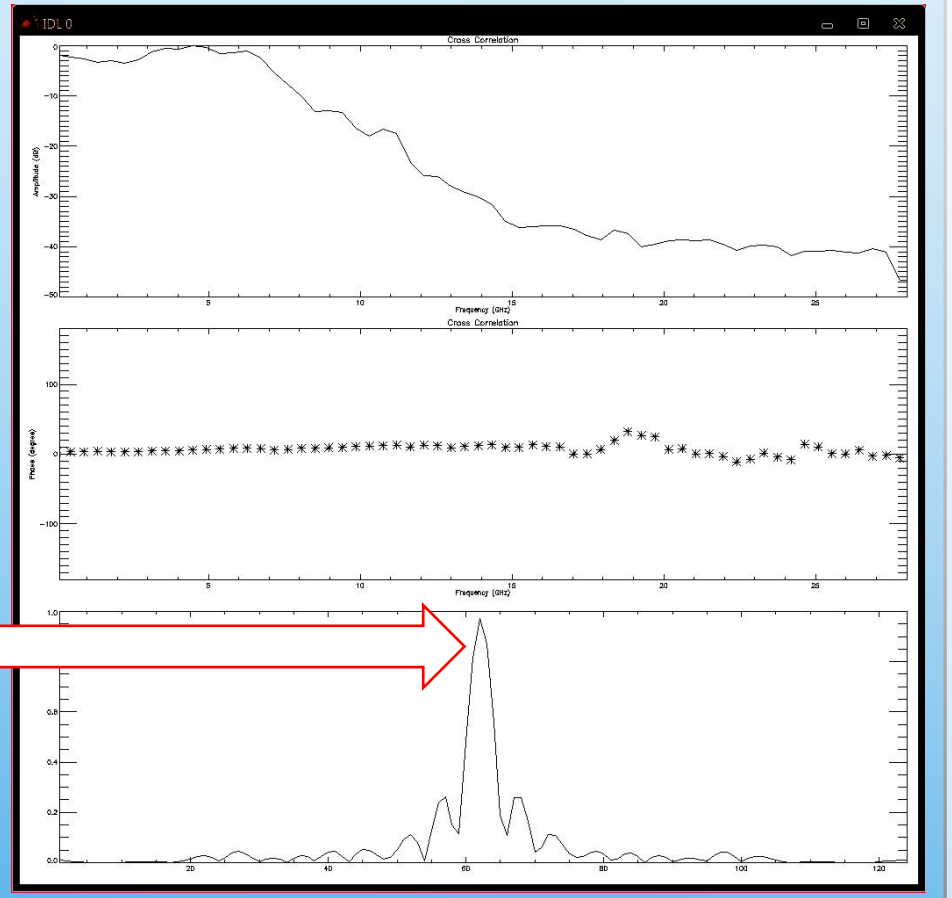
Total sample rate 112 Gsps @8bit on a single chip (2 options)

- 2 x 56 Gsps
- 4 x 28 Gsps

Effective bits: 6.5

Output: via 96 high-speed parallel lanes

Assembly of the the 96 output lines into a valid, fully-sampled data stream by 4 on-board FPGAs.



Zero-baseline fringe over the full band 0-28 GHz

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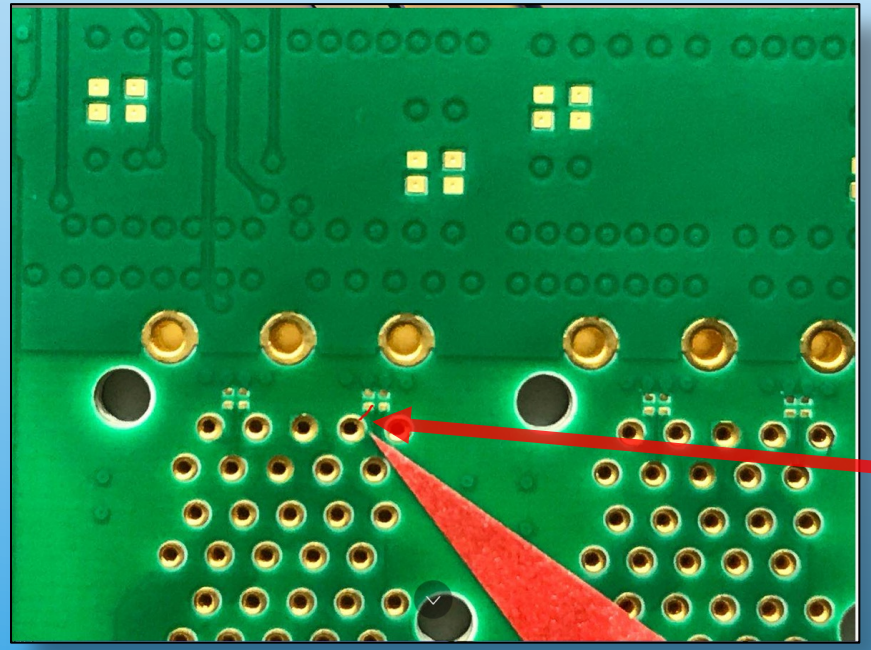
BRAND ISSUES - PCB

Production of PCB board by Chinese manufacturer

- Challenging due to large size, large number of layers, high-currents
- Production of 6 boards: 1 x functional, 1 x minor defects (fixed), 4 x defective



Etching issue (missing lane)

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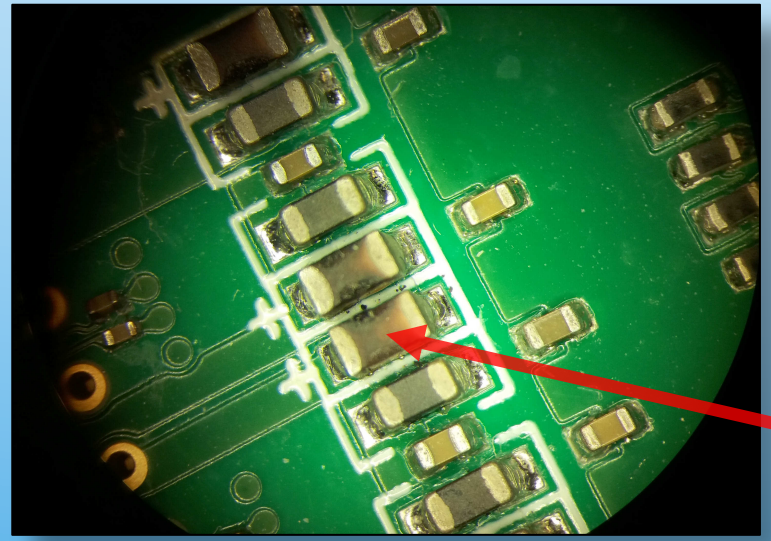
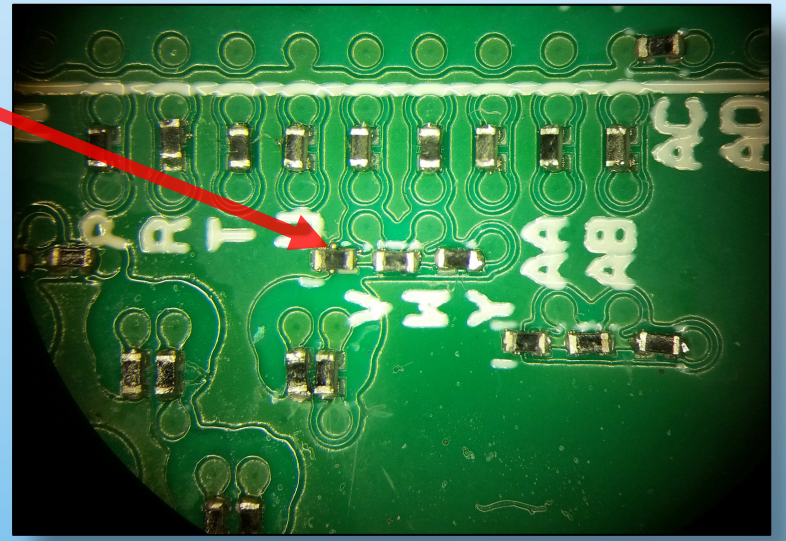
BRAND ISSUES - PCB

Soldering issues found (could be fixed in-house):



Overheating in some areas of the PCB

Underheating in some areas of the PCB



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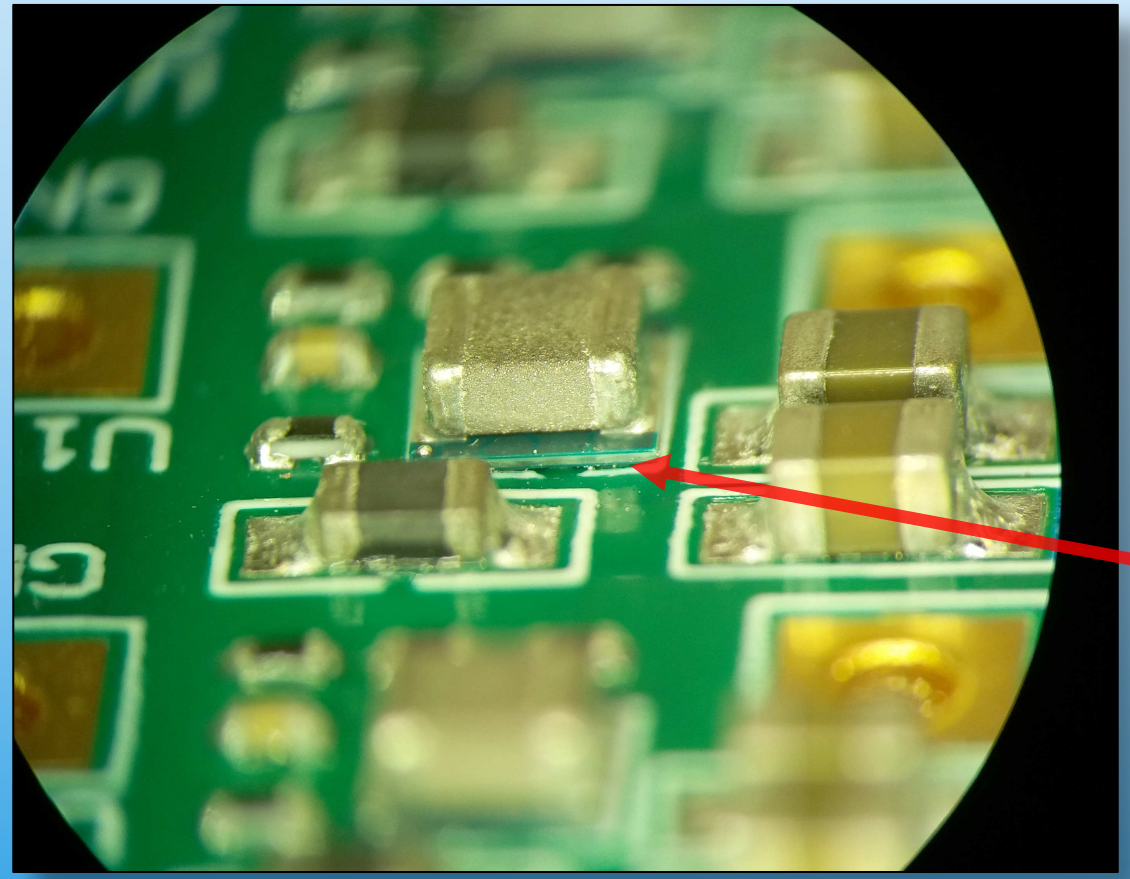
BRAND ISSUES - PCB

Soldering issues due to uneven solder mask (fixed in-house):



Tilted power-regulators due to uneven solder mask surface

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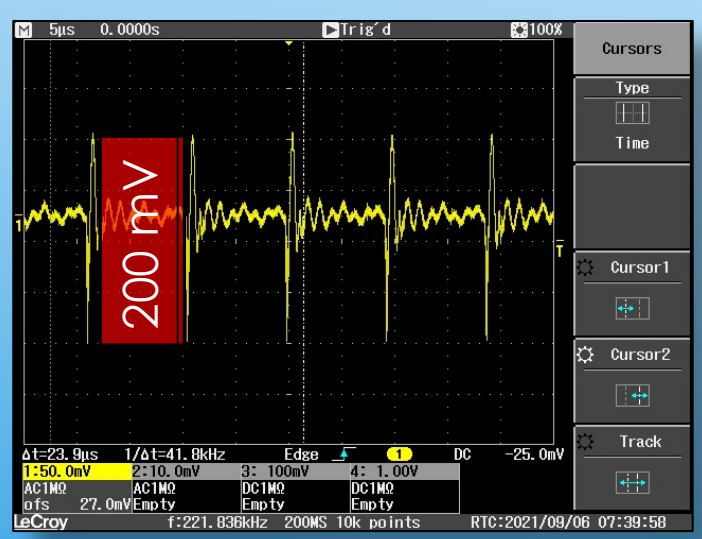
BRAND ISSUES – POWER SUPPLY

PCB power requirements:

	current	voltage
FPGA	Max. 100A	0.95V
Sampler	Max. 16A	1.25V
High-speed data lanes	Max. 12A	1V



Required voltage stability: < 10mV peak to peak

Not met by original design!

Issues:

- Sampler reset
- FPGA programming lost

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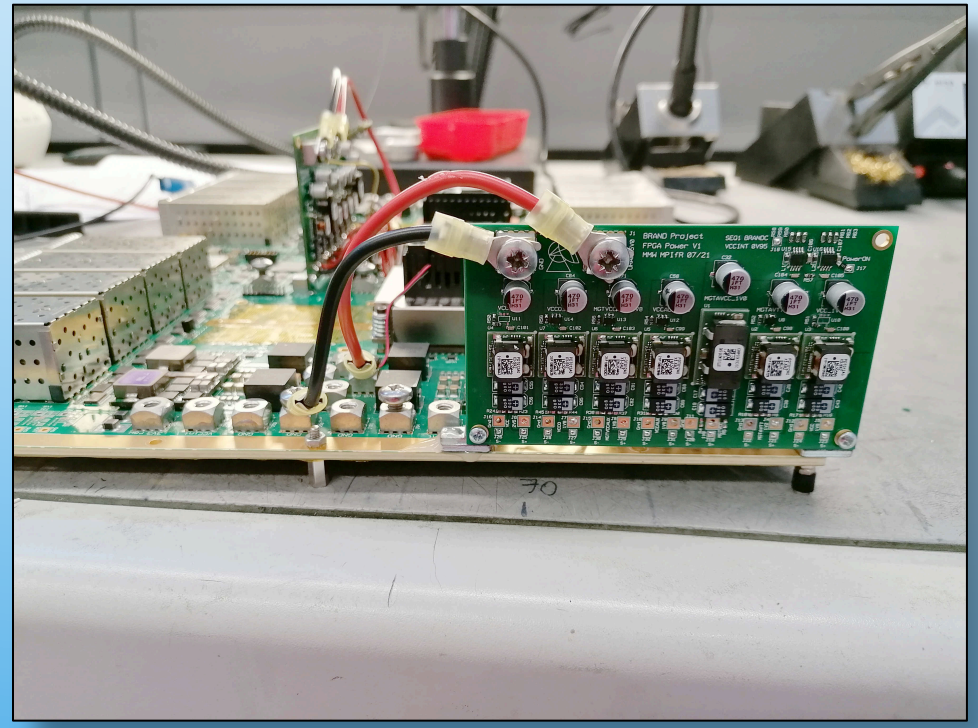
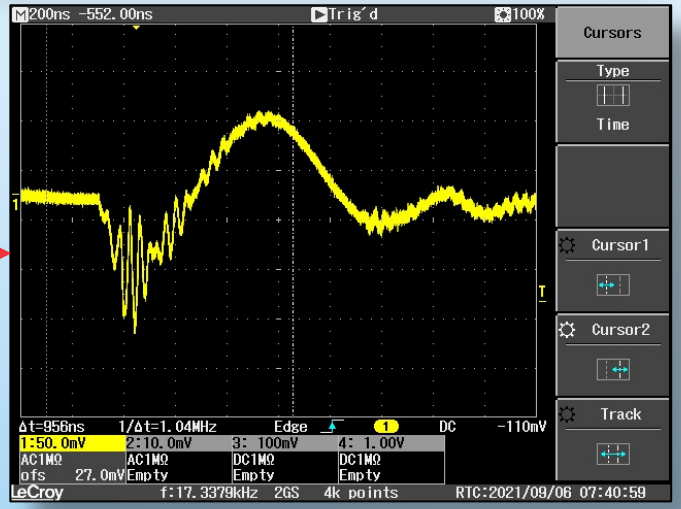
BRAND ISSUES – POWER SUPPLY

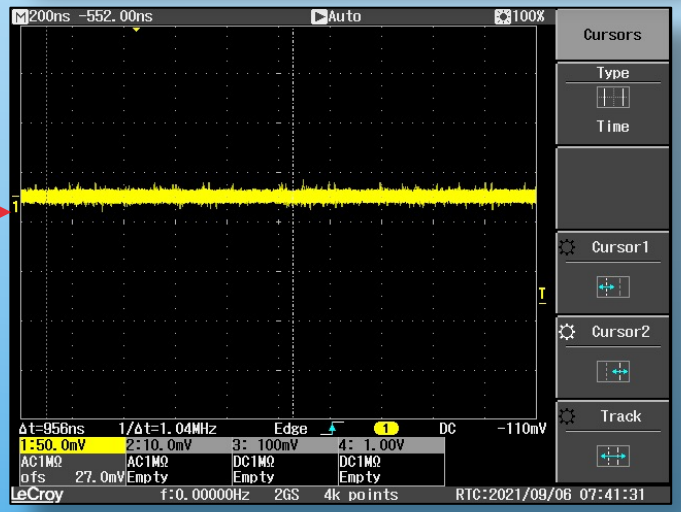
Redesign of PCB power supplies



Original power supply



Reworked power supply



Stable operations of sampler and FPGA after fix

BRAND ISSUES: SYNCHRONISATION

Issue: Data arriving on the data lanes from the sampler to the FPGA was recognized as „*invalid*“ by the FPGA transceivers.

Issue very difficult to diagnose without the proper equipment.
Since July 2021: 40 GHz sampling scope

- Considerable progress in understanding the problem (eye pattern)
- Error in the PLL synchronization of the sampler threads

Code is fixed and “valid” data arrives at the FPGA transceivers over all 96 lanes.

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BRAND STATUS & OUTLOOK

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Next immediate steps:

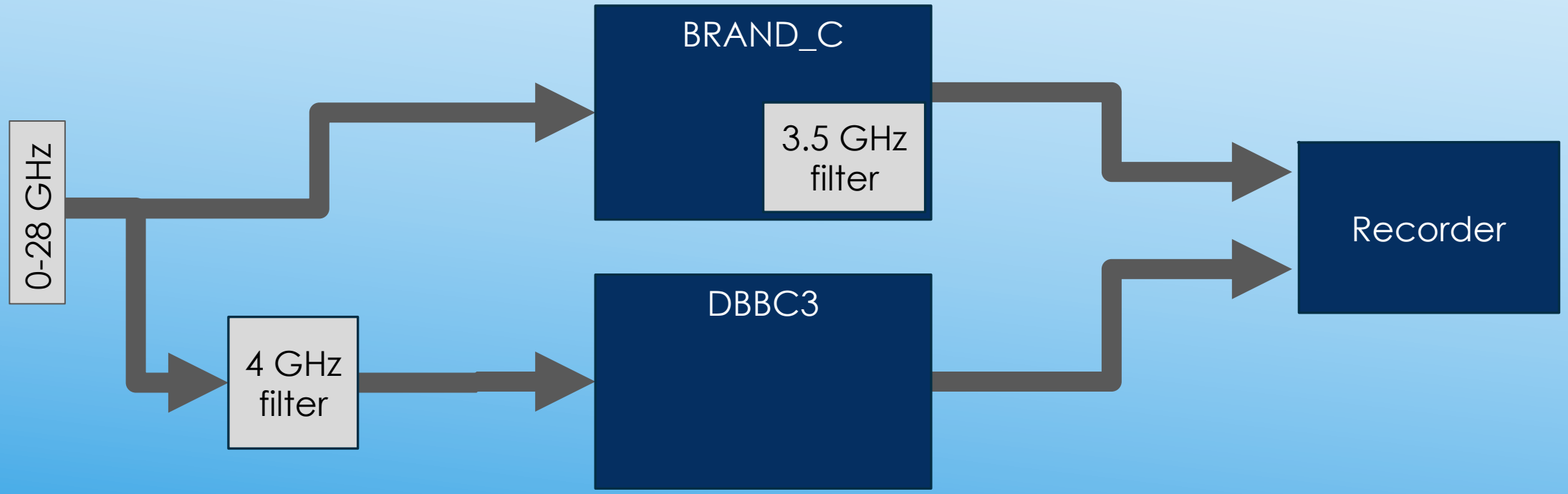
- **Finalisation of BRAND FPGA firmware:**
  - Channelisation into 3.5 GHz sub-bands
  - VDIF packetizer
- **Finalisation of DBBC3 firmware:**
  - Bi-directional operation of Core3H transceivers
- **Zero-baseline fringe verification** of recorded VDIF data
  - DBBC3 with two digital input streams from the BRAND digital frontend

Milestone (end of march):

- Simplified Zero-baseline test between BRAND and DBBC3

MILESTONE ZERO-BASELINE TEST

Simplified zero-baseline test planned before end of March



BRAND SAMPLER ORDER

Delivery of sampler chips declined by manufacturer in 2021
- Minimum order quantity: 30 units
- EVN orders (via MPIfR): 11 units

Update:
- Money for ordering additional sampler chips secured within the DBBC4 project (MPG)
- Place order after successful lab tests
- MPIfR will contact partners again in spring/summer 2022