DBBC DEPLOYMENT: STATUS JUNE 2019

DBBC2

DBBC1 Noto (later updated to DBBC2)

DBBC1 Wettzell1 (later updated to DBBC2)

DBBC1 Wettzell2 (later updated to DBBC2)

DBBC1 Wettzell3 (later updated to DBBC2)

DBBC2 Effelsberg

DBBC2 Yebes

DBBC2 Auscope1 (Hobart12M)

DBBC2 Onsala1

DBBC2 SRT

DBBC2 Pico Veleta

DBBC2 APEX

DBBC2 Wark12M

DBBC2 Auscope2 (Kath12M)

DBBC2 Auscope3 (Yarr12M)

DBBC2 Torun

DBBC2 Irbene1

DBBC2 Hartebeesthoek1

DBBC2 Hartebeesthoek2

DBBC2 Auscope4 (Ceduna)

DBBC2 Medicina

DBBC2 Metsahovi

DBBC2 Auscope5 (Hobart26)

DBBC2 Tianma

DBBC2 Warkworth2 (New Zealand)

DBBC2 AVN (Ghana)

DBBC2 Ny Alesund

DBBC2 Onsala2

DBBC2 Yebes2

DBBC2 Jodrell Bank

DBBC2 Yebes3

DBBC2 Wettzell4

DBBC2 Westerbork

DBBC2 Warkworth3 (New Zealand)

DBBC2 Shanghai

DBBC2 Urumqi

DBBC2 SRT2

DBBC2 Irbene2

DBBC2 Kunming

DBBC3

DBBC3-4L4H Upgrade APEX

DBBC3-4L4H Upgrade PicoVeleta

DBBC3-6L6H Hobart

DBBC3-2L2H Yebes

DBBC3-8L8H Onsala1

DBBC3-8L8H Onsala2

DBBC3-8L8H Ny Alesund1

DBBC3-8L8H Ny Alesund2

DBBC3-2L2H Effelsberg

DBBC3-2L2H Sejong (NGII)

DBBC3-6L6H Katherine

DBBC3-6L6H Yarragdee

DBBC3-8L8H Wettzell1

DBBC3-8L8H Sheshan

DBBC3-8L8H Methsahovi (FGRI)

DBBC3-4L8H Torun

DBBC3-2L2H Bonn

DBBC3-4L4H Tianma

DBBC3-2L2H Wettzell2

DBBC3-8L8H Wettzell3

Red under construction

DBBC2 FIRMWARE DEVELOPMENT

- **DDC v107**
  Input bwd: 512 MHz (in the range 0-3,5 GHz)
  4 bbc/Core2
  Output bwd: 128 – 64 – 32 – 16 – 8 – 4 MHz
  U & L (8 channel)
  Complete and under observation test

DBBC3 FIRMWARE DEVELOPMENT

- **DDC v125_Ux**
  Input bwd: 4096 MHz (in the range 0-15 GHz)
  12 bbc/Core3H
  Output bwd: 128 – 64 – 32 – 16 – 8 – 4 MHz
  U & L (32 channel)
  Complete and under debug
  Observation test possible at the debug completion

- **DDC v125_Uz**
  Input bwd: 4096 MHz (in the range 0-15 GHz)
  16 bbc/Core3H
  Output bwd: 128 – 64 – 32 MHz
  U & L (32 channel)
  Complete and under debug
  Observation test possible at the debug completion

- **PFB v100**
  input bwd 4096 MHz (in the range 0-15 GHz)
  64 channels
  output bwd: 64 MHz
  U or L
  Developed for the initial DBBC3 version
  To be adapted at the new implementation