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Description and evaluation of the digital part of the BRAND receiver (backend)

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Dissemination Level

Dissemination Level		
PU	Public	X
PP	Restricted to other programme participants (including the Commission Services)	
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CO	Confidential, only for members of the consortium (including the Commission Services)	

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1 Elucidation

COVID-19 affected the Deliverable D6.3, to which the Art.51 applies as follows: Description and only partly evaluation of the digital parts of the BRAND receiver (digital backend and digital frontend) have been achieved. A full evaluation of the entire digital part of the BRAND receiver (backend) will be done after RadioNet in Q1/2021 and Q2/2021 depending on the restrictions implemented in Italy and Germany in the next few months. In particular travel restrictions affect the collaboration on the digital parts strongly.

2 Introduction

The BRAND receiver analogue frontend presents at its output an instantaneous bandwidth of 14 GHz in both polarisations. Traditionally such a wide band has been cut into more manageable pieces by the use of analogue filters and mixers, because the width of samplers was quite limited in the past, in particular if at least 8 bits of sampling depth were required to have enough dynamic range in view of-ever increasing Radio Frequency Interference (RFI).

For VLBI, the use of different mixers destroys the phase relation between different parts of the band, which makes coherent integration over wider frequency ranges at least difficult. The recent increase in bandwidth to 4 GHz, which a modern VLBI backend like the DBBC31 offers, has removed some of the limitations already. With BRAND, now this limit will be pushed to 14 GHz which is more than the total bandwidth that the EVN offers in its most requested frequency range between 1.6 GHz and 8.5 GHz, though with a multitude of narrow-band receivers not simultaneously available, and with a varying mileage with regard to characteristic parameters like bandwidth. In addition to covering in principle the frequency gaps between the available receivers, the 15 GHz band could be offered as a standard EVN frequency via BRAND receivers. Altogether this very wide band can be stitched together more easily due to the single sampler approach, and the total sensitivity will be increased.

Another strong argument for the BRAND concept is that it can also serve as a second-generation VGOS receiver. Without mixers, forming a so-called multi-band delay – the primary observable for geodesy – would be simpler, more reliable, and more precise.

The outstanding results achieved for the analogue components of the receiver require similar efforts in the digital domain. A key element in the success of finally implementing 14GHz-wide sampling, band selection, VLBI formatting, recording, and correlation has been the Quad 8-bit 56 GSps ADC chip not generally available on the market. We could acquire this chip for our project with an agreement, which includes a purchase option for at least the EVN stations.

[1]DBBC3: developed by JRA DIVA of RadioNet3 (EU contract 283393)

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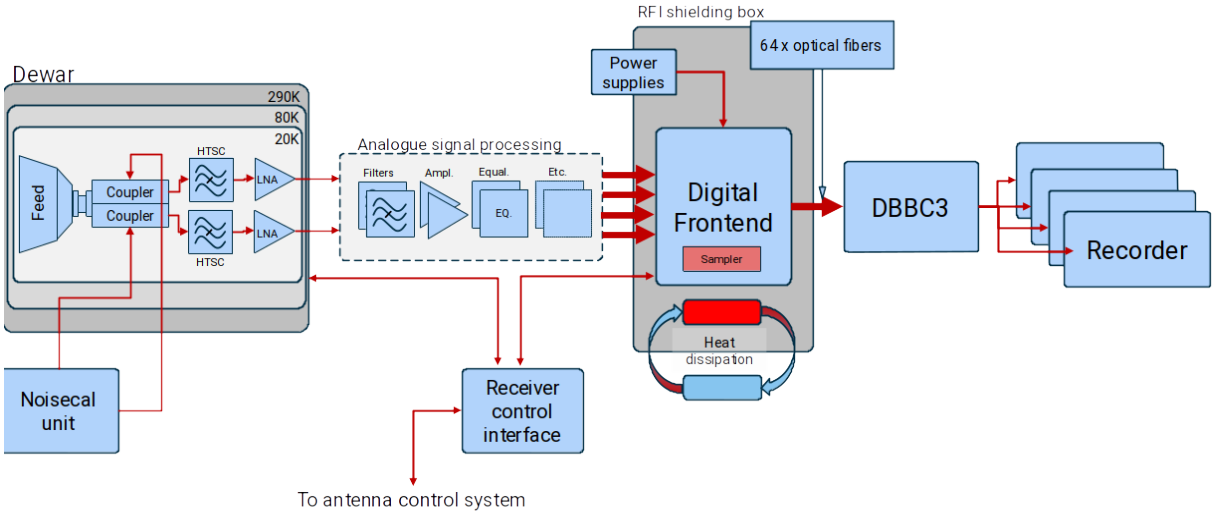

Figure 1: BRAND receiver block diagram. From the feed up to and including the digital frontend each component is located in the receiver frame. The DBBC3 backend and the recorders are located close to the control room.

The digital part of the receiver starts with the digital frontend (DF). This component was originally thought to reside in close location to other backends far from the receiver in the focus of the antenna. In the proposal and contract phase we still believed that we could transport the analogue signals to the backend room over optical fibres (RF over fibre). This method was evaluated at Effelsberg and only later it was found that the dynamic range of the analogue fibre link is too small for radio astronomical signals, which also carry a strong RFI component. This triggered the development of digital frontends to be situated in or close to the receiver.

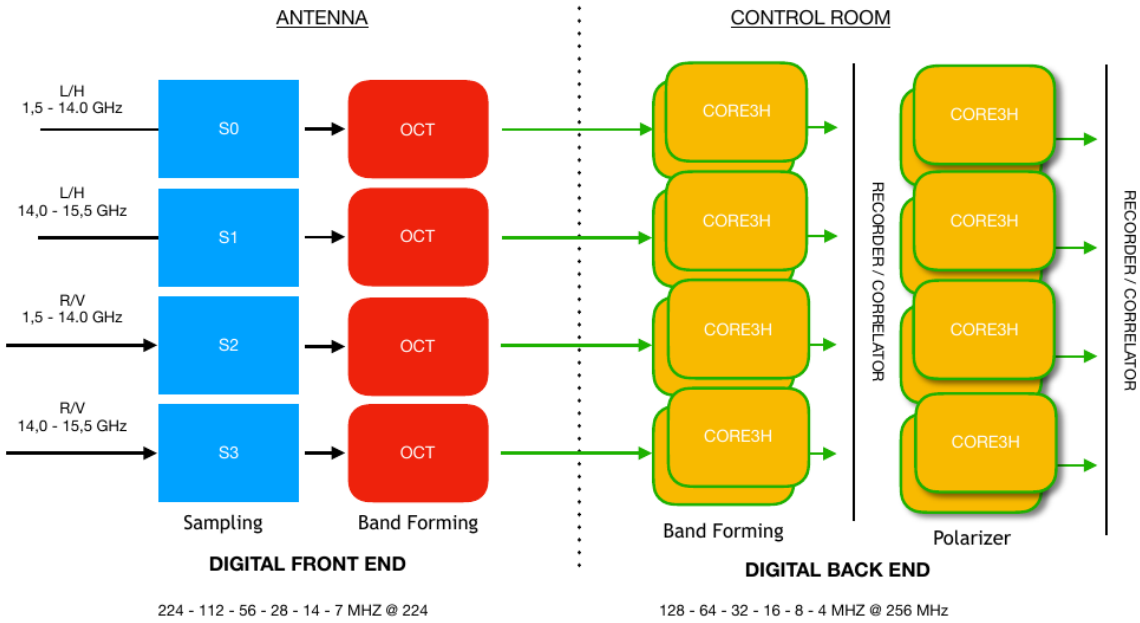

Figure 2: Signal flow in the digital part. From the left the four analogue signal streams enter the samplers in the sampling chip. Next the data is received, combined to bands, and filtered into the desired wider output bands. The digital data is then sent to the digital backend DBBC3 where VLBI sub-bands are formed and optionally the polarisation is converted into circular polarisation.

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This change in planning meant additional research had to be done to dampen the RFI induced by the BRAND DF itself by about 120 dB. This can only be achieved by surrounding the DF board by one or two specially developed aluminium boxes. At the same time the cooling of the sampler chip (ADC) and FPGAs, which is needed for the initial band selection, has become much more demanding due to the extreme encapsulation. The design of the housing of the BRAND DF will start as soon as the level of RFI the BRAND board generates can be measured.

The DF board itself needs to be as compact as possible while at the same time it has to carry about 1 Tbps from the sampler to the FPGAs which are needed to make this enormous data rate transportable over 10GE optical fibres (requirement imposed by the DBBC3 backend).

The DBBC3 backend is just powerful enough to receive the amount of data generated by the DF. The advantage of using the DBBC3 for this purpose is that it is a stable, well debugged backend with the required firmware for generating standard VLBI sub-bands and output. Its FPGA processing board (Core3H) had been designed during the previous RadioNet such that a total of eight SFP+ Ethernet connections can be handled per board. A total of eight Core3H boards can be installed in a DBBC3.

Further processing of the BRAND digital data is described in the report for the deliverable D6.4.

3 Digital Frontend

Shortly after the start of the BRAND project it became clear that we would be able to procure sampling chips with four sampling cores, each of which can handle up to 14 GHz of bandwidth on input. This matches ideally the BRAND band of 14 GHz width from 1.5 GHz to 15.5 GHz.[2]

The characteristics of this sampler chip and the chosen backend DBBC3 define the layout of the digital frontend board. The DBBC3 uses 10 GE technology for data output, but it was foreseen during the development that the up to eight transceivers of each processing board of the DBBC3 can also work as data input.

The sampler chip generates on output about 1 Tbps of data. It was estimated that this can be handled with four big Xilinx Kintex Ultrascale FPGAs. Another boundary condition is the space available in the receiver frame and dissipation of the heat created by the four big chips and the Ethernet transceivers.

3.1 Hardware

The BRAND digital frontend is an innovative concept for a radio-astronomy receiver implementation. The functionality traditionally performed in the analogue domain is here shared with numerical operations in the digital domain. In order to allow this, a very ambitious analogue to digital conversion is required at the RF level rather than IF. This requires operating at very high clock rates when the entire wide band (28 GHz) is to be handled.

On the other hand working at half band is still suitable for the BRAND application because the bandwidth is just 14 GHz, even if crossing the first Nyquist zone. So a possible solution to operate at half band is to prepare two bands, 0-14 GHz and 14-15.5 GHz and use two sampling channels per polarization, having available four independent inputs at half data rate as an alternative to two independent channels at full data rate. Thus the solution of using four channels was adopted and the analogue part developed to produce two separate frequency ranges as described above. In the course of the digital development it became clear that also the full data rate option can be safely implemented, and so both options are kept available in the digital data path for future use.

[2] Alternatively the chip can sample 2 x 28 GHz of bandwidth at 56 GSps, which we could verify.

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The BRAND_C board – the main component of the digital frontend – thus has available four differential input channels, which are fed by four broadband (20 GHz) baluns. Feeding the input with the differential version of the analogue signal is indeed a preferred solution to optimise the noise performance of the sampler.

A deep characterization of the samplers was conducted at an earlier stage, and it was decided to adopt this sampler for the BRAND project. Here we report some elements of this characterization.

The sampler device is developed as ASIC (application specific integrated circuit) and is much more than a pure sampler device, indeed it can be considered as a very complex processor with a capability to handle four channels of broad-band analogue signals for numerical operations with output at full data rate with two channels in the real domain, or four channels half rate in the complex domain with a nominal 8-bit representation.

The actual sampling operations in the chip are then organized in a flexible fashion using very fast quad-interleaved samplers to produce a set of different digital representation of the two or four analogue signals.

Interleaved sampling requires careful balancing of mainly three different elements to produce a useful set of data with minimal artefacts: gain, offset and delay between the different elements of the samplers. This implies dedicated strategies to set and maintain the correct relation between the sampling elements. This is a general requirement, and in the device it is accomplished by a dedicated logic and set of registers, which can be managed internally appropriately driven by an external controller.

Relevant item is the actual working frequency, which requires a complete synthesizer internally to the device that is in phase lock with an external frequency reference. All the low noise multiplications are performed and controlled internally in the device, greatly simplifying the operations and the above described calibration.

A number of mathematical operations can be selected in the chip for single channels or a combination of them. As becomes obvious the device is not only a sampler, but a data rate processor, too.

After the desired data handling is performed the selected data can be transferred to output, again with a combination of flexible options, at the full data rate or with a reduced version of the sampled data. The output operation is performed by a wide number of output transceivers adopting a semi-standard network protocol. Any further use of the produced data is realized by coupling to a number of FPGA or ASIC devices capable of handling the very high output data rate (about 1 Tbps).

In order to validate this high performance device a number of measurements have been executed on a real device. As described it offers a wide range of possible implementations, and so in particular we concentrate here on the main elements which could be considered useful in the frequency domain up to a maximum of 16 GHz, even if the actual complete bandwidth with reduced performance is much wider (28 GHz). With ‘reduced performance’ we mainly consider the total effective number of bits for representing the analogue input signal.

Many measurements have been done using the prototype board procured for the initial testing phase, and in one of the laboratories of the company producing the device. Here we report the main ones which can have an impact on the performance of a VLBI receiver, and which could be obtained with the available equipment. The device requires a number of voltages with high current as well as different frequency references and control software for interfacing the device for operating the calibration of the samplers and mode settings.

The results of our preliminary measurements which are here reported are not a full evaluation – this will only be possible with a dedicated receiver placed in one of our radio-telescopes –, but for sure deserve high regard and further research due to the good and very promising performance which has been found. The BRAND EVN project itself is in some way a consequence of the existence of this device and of the next generation of similar devices

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developed with the same or similar technology.

The tables below report different sets of measurements. The ENOB (Effective Number Of Bit) was determined as a function of frequency at about 25 °C.

Frequency (GHz)	ENOB
1	5.95
2	5.89
3	5.87
4	5.82
5	5.89
6	5.91
7	5.91
8	5.92
9	5.92
10	5.91
11	5.88
12	5.90
13	5.87
14	5.88
15	5.89
16	5.99
17	6.01

The values reported in the table are calculated from the relation ENOB as a function of SINAD (power ratio between useful signal + noise + distortion and noise + distortion).[3]

The sampler device is able to operate in a broad temperature range (-40 / +110 °C). Due to the relatively high power dissipated in the chip (strongly dependent on the resources used in the processor) we could face high junction temperatures. Therefore we measured the ENOB as a function of temperature. In the table below the measured average reduction in the number of bits at different temperatures of the device at 12 GHz can be seen.

Temperature °C	ENOB Reduction
25	0.00
35	0.01
45	0.02
55	0.02
65	0.03
75	0.04
85	0.06
95	0.08
105	0.10
115	0.13
125	0.17

Additional ENOB measurements have been taken with respect to the reduction of the input level with respect to the full scale value. The table below reports these data at 12 GHz. These types of measurements are useful because they could help to determine the best operative input level range of the sampler, which mostly typical for the technology adopted for the fabrication of the device.

Reduction (-dBFS)	ENOB
25	5.88
20	5.94
15	6.20

[3] For a definition see: https://en.wikipedia.org/wiki/Effective_number_of_bits

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12	6.18
9	6.01
6	5.78
3	5.40

Finally the bandwidth at about 25 °C was measured as level reduction function vs. frequency. The table below reports the value determined using a signal at -6dBFS.

Frequency (GHz)	Level (dB)
1	-0.2
2	-0.5
3	-1.0
4	-1.1
5	-1.1
6	-1.1
7	-1.3
8	-2.0
9	-1.5
10	-2.0
11	-2.0
12	-2.2
13	-2.5
14	-2.5
15	-2.9
16	-3.2
17	-3.5

Using two identical prototype boards it was possible to acquire data synchronized with a start trigger pulse in order to perform a cross-correlation of the data stream.

A commercial broad band noise generator was not available, and so a noise source was assembled with a number of broad band amplifiers. In this solution the noise of a single amplifier is multiplied. The bandpass is typically affected by a frequency slope decreasing the output level at the higher frequencies. With this not ideal noise source generator a number of acquisitions have been done and an example of the results is shown below (see Fig. 3). The cross-spectrum is shown as amplitude and phase over 14 Ghz. Additionally a single tone at 14 GHz in the entire 28 GHz full spectrum, in which the device is able to operate, is shown in cross correlation (see Fig. 4).

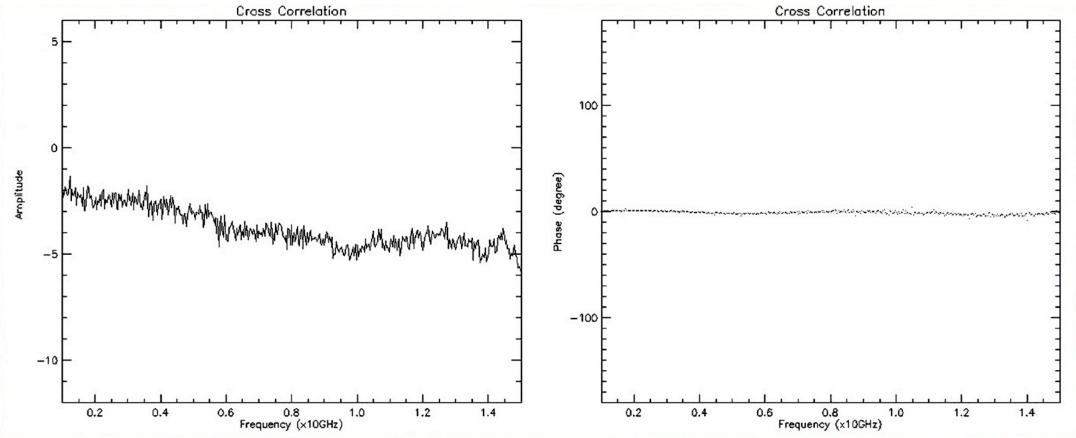

Figure 3: Correlation amplitude and Phase of a 16 GHz continuum signal. The correlation was performed between two evaluation boards of the wide-band sampler.

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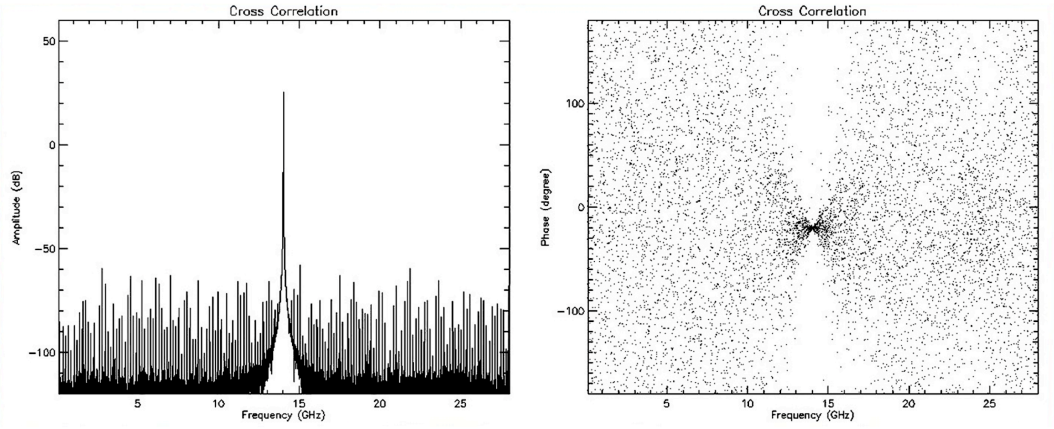

Figure 4: Correlation amplitude and phase of a line signal at 14 GHz inserted in the 28 GHz analogue input signal.

The main part of the digital frontend of the BRAND prototype – called DiFrEnd – are the BRAND_C board[4] (see Figs. 5, 6, 7), a small fan-less PC for supporting the control operations, and a number of remotely controllable PSUs (power supply units). The communication between the general control software and the digital frontend is performed using a network socket for general and simplified operations, while the communication between the small PC and the BRAND_C board is accomplished with a number of USB connections.

The control channels are USB ports and have the tasks to:

a) Communicate with a Spartan3 FPGA utilised to talk to the sampler device for all the functions it supports, to the two synthesizers the sampler device requires as clock sources, to a number of A/D converters to monitor the large number of voltage rails required
b) Control the internal voltage regulator sequence needed to power the different sections of the board
c) Control additional synthesizers for calibration and general use
d) Communicate with the processing FPGAs

The interfaces implemented to handle the USB communication belong to the FTDI family and allow a number of options for programming. In particular two types of them are used: one for operating a synchronous data bus and another for emulating a four-channel RS232 interface. The first type is used for the dialogue with the Spartan3 device which manages a large part of the interface operations with the sampler device, the ADC samplers for monitoring the voltage rails powering all the critical devices in the board, and for programming the four synthesizers. The RS232 interfaces are used for talking to the four FPGAs when on-the-fly programming is required.

[4] In the final version it is going to be named COREagle.

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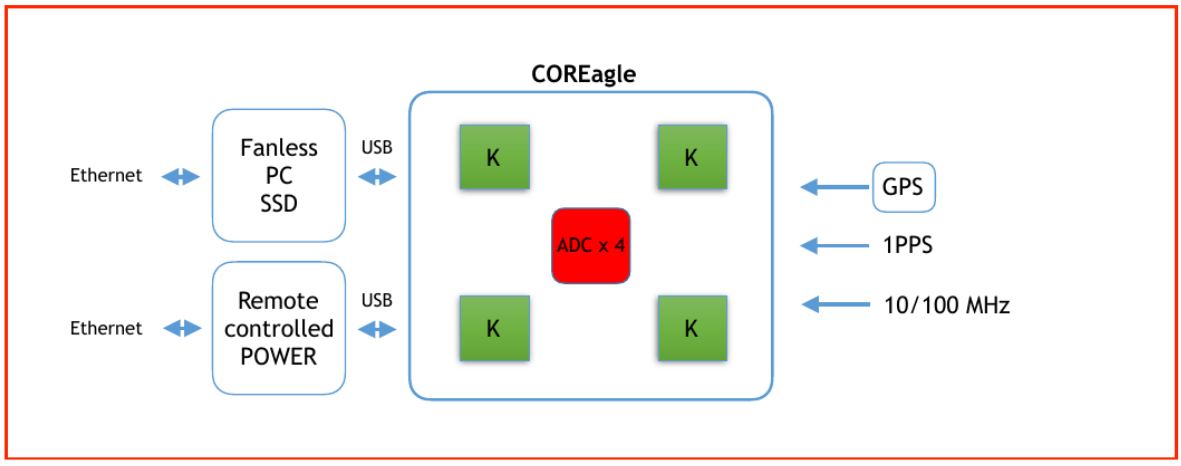

Figure 5: Simple block diagram of the BRAND_C board. K = Kintex Ultrascale FPGAs.

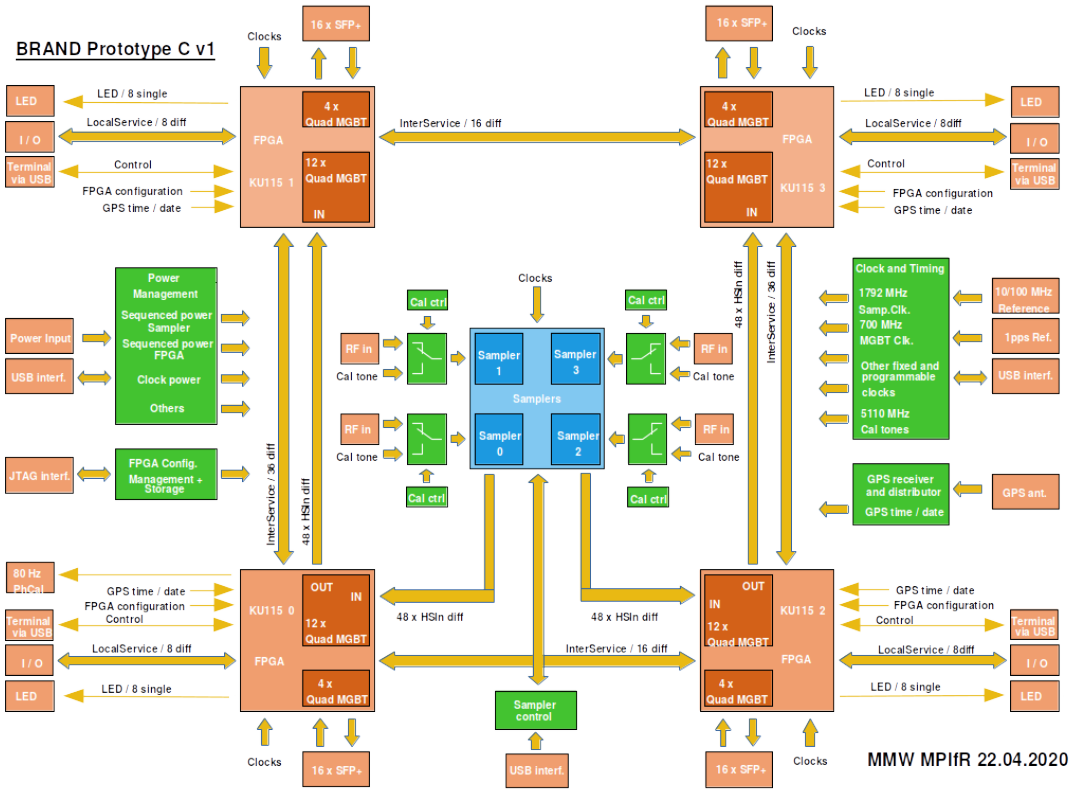

Figure 6: Block diagram of the digital frontend board. The sampler chip is seen in the centre in blue. The four FPGAs receive the data from the sampler and send it to the SFP+ connectors. The FPGAs are also connected with each other, so data can be forwarded between them.

The BRAND_C board (see block diagram in Fig. 6 and populated board in Fig. 7) is built around the broad-band sampler chip described above which can work like four full rate (56 GSps) 8-bit samplers. It can also perform a large number of functions to finally form the sampled and pre-processed data, select, and transfer a maximum of about 1 Tbps of it using 96 fast lanes, operating in 10G-KR regime, to four Ultrascale Kintex Xilinx FPGAs. In the sampler four channels can be used at half rate (28 GSps) or two channels full rate (56 GSps).

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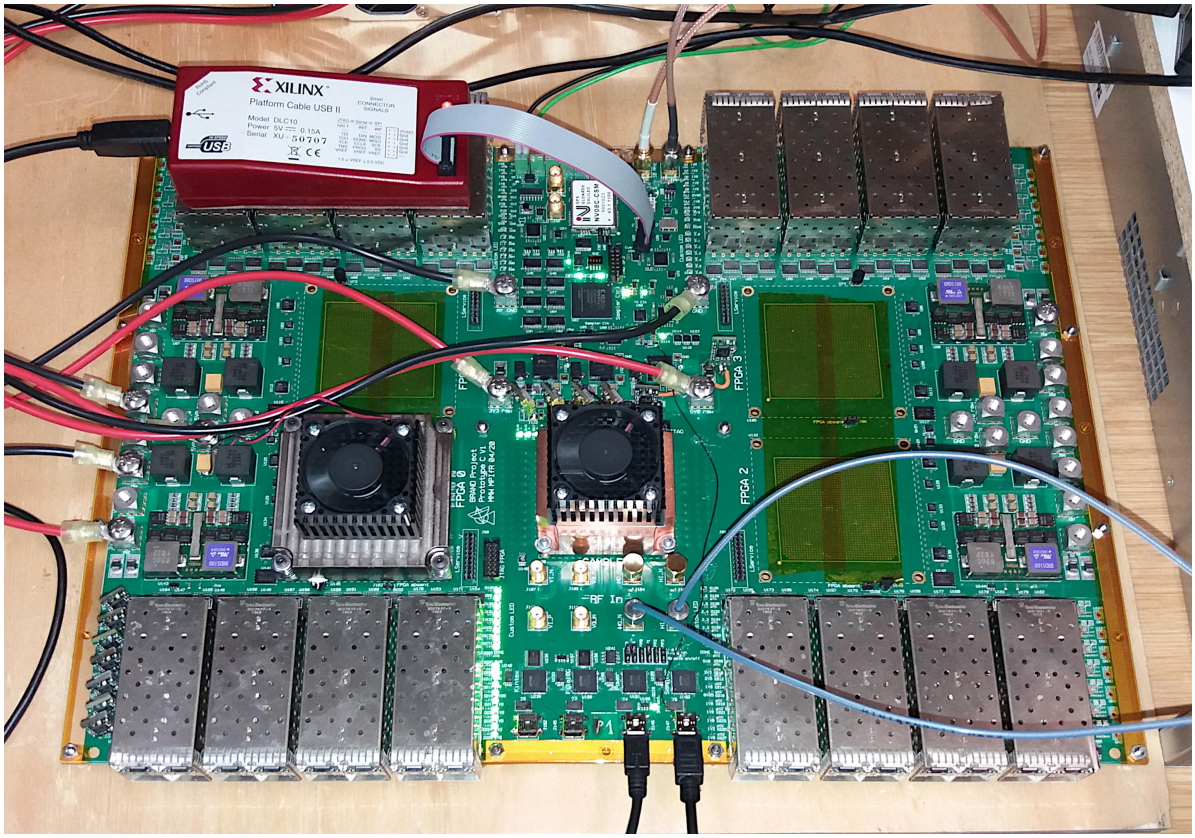

Figure 7: Populated prototype board BRAND_C. The sampler chip with a fan for cooling is seen in the centre. The lower left of the four Kintex FPGA sockets is populated. The small Spartan3 FPGA is seen on the top centre of the board just above the black cable.

In particular 48 lanes for one/two sampled channels are routed to two of the FPGAs, while the same data is forwarded to the two additional FPGAs for dealing with the same information, but to perform a different process.

The FPGAs are used to execute the initial band filtering with OCT techniques[5], and anything required at this stage (total power, continuous calibration modulation, etc.). The selected portions of band are then formatted as required by the VLBI method. The data are encapsulated in standard 8-bit multiplexed VDIF 10GE packets and forwarded to the digital backend using eight transceivers per sub-band to illuminate the same number of optical fibres, which transfer the information to the digital DBBC3 backend.

The full DiFrEnd can be seen also as a black box with external connections:

a) Two full rate or four half rate broad band analogue input
b) Station frequency and time reference signals: 10 MHz, 1PPS
c) GPS active antenna input
d) Continuous calibration synchronism
e) 1 Gbps Ethernet connection
f) 64 optical fibers
g) 230V Mains

[5]OCT is a flexible filter with arbitrary band selection within the input band by using one or two digital FIR-filters.

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3.2 Preliminary testing of the hardware

Due to the delays in the project caused by COVID-19 only some preliminary, but nevertheless very promising tests could be conducted. While the aim for the laboratory tests is to perform extensive zero-baseline correlations between the two boards which were manufactured for the project to investigate the response of the BRAND_C board, we could only do one first test between two independent samplers in one sampling chip.

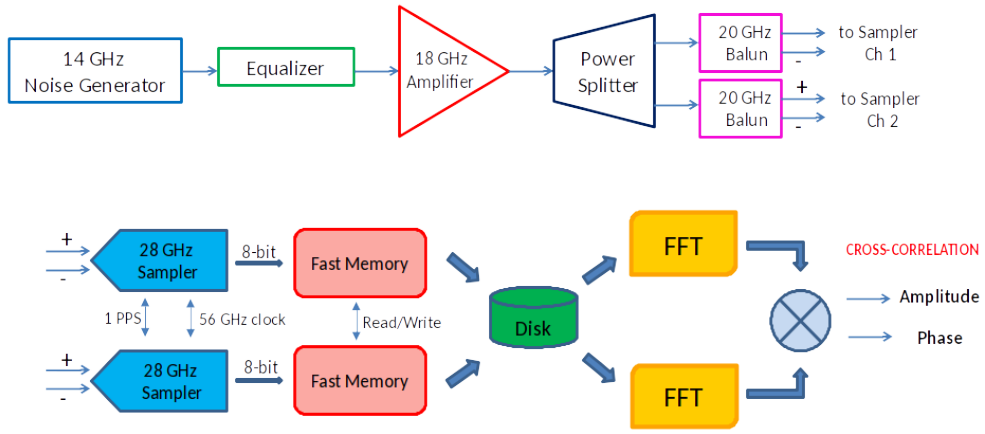

Figure 8: Zero-baseline fringe test: schematic view

In this first of a series of laboratory tests to evaluate the performance of the sampling process of the BRAND board for VLBI applications the capability of the broad band samplers to maintain good phase stability should be investigated for the entire frequency range where the receiver has to operate, that is between almost zero up to 16 GHz.

Such a type of evaluation is normally performed with the so-called zero-baseline cross-correlation test using as signal source broadband Gaussian noise. In our laboratory we have a noise generator, which is able to produce this type of noise. Even though the noise has no normalized amplitude, it is still well suited to evaluate the performance of the sampler device and the BRAND board in the entire operating frequency range.

In the figure 8 schematically the entire environment test can be seen. The noise source produces broad band noise with an amplitude decreasing with frequency. In order to mitigate this effect and improve the amplitude slope a frequency equalizer was introduced before a robust amplification stage to get sufficient power in the entire spectrum of interest.

The broad band noise signal is then split into two identical parts which is required for comparison of amplitude and phase after the conversion to the digital domain. Two independent samplers inside the sampler chip on the BRAND board are then fed by a 20 GHz differential power splitter to drive the analogue to digital conversion process using a highly stable 56 GHz synthesized clock (four-phases interleaved 14 GHz) in synchronism with a 1PPS (one pulse per second) signal.

The two high-rate data streams, represented by 8-bit samples at full clock rate (448 Gbps each) are recorded in parallel on a dedicated fast memory bank internal to the sampler device. After the acquisition this data can be read out from the memory at a much slower rate so that it can be written to the disk of a computer, which manages the acquisition operations.

The resulting data files can then be processed by a correlation software which extracts the two streams and performs the required operations to cross-correlate them in FX fashion. Finally the amplitude and phase of the cross-correlation are calculated and represented in plots as a function of frequency.

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In the plots of figure 9 the result of our measurement is reported. The correlation amplitude of the two samplers is in the range 95-98 % which represents an excellent value for VLBI applications. The correlation is even good for the highest possible frequencies. As can be seen in the phase plot the correlation exists up to 28 GHz (the maximum frequency the sampler can support) where the input noise level is very low, and which is well beyond the maximum frequency of 15.5 GHz at which the BRAND receiver will operate.

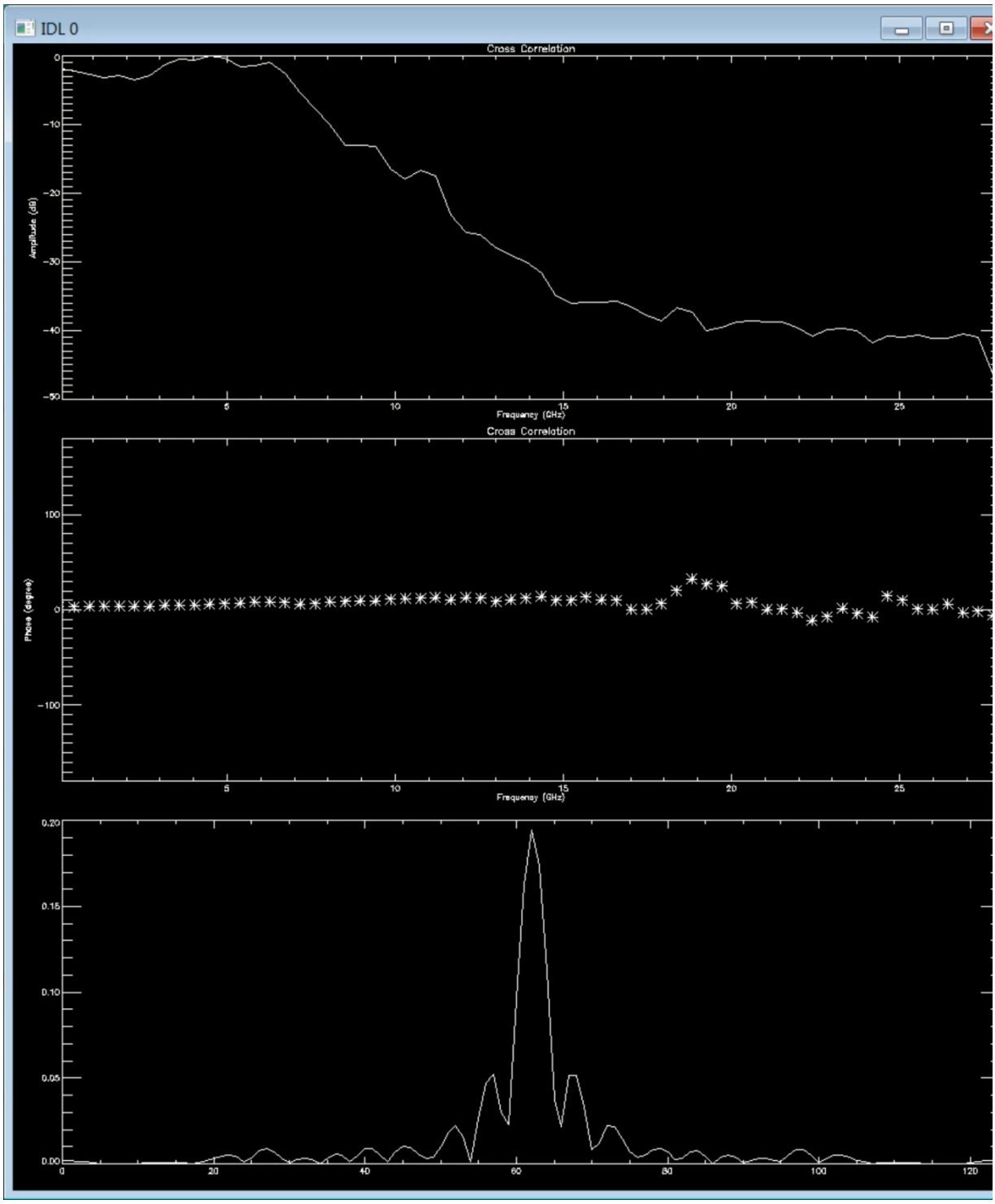

Figure 9: Zero-baseline correlation results. In the top plot the input frequency spectrum can be seen. In the phase plot in the middle can be seen that the interference signal can well be detected up to 28 GHz. The phase fluctuations at the higher frequencies indicate a low noise level of the fringes as expected from the low input signal. Also the amplitude plot at the bottom shows a very strong fringe due to the identical noise fed to both independent samplers.

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More cross-correlation measurements will be made in the future with varying thermal noise added to the signal. The tests will also include additional stages of the receiver which are more traditional like the DBBC3, widely tested in other VLBI systems. The broad band sampler is the very new and most critical element in the digital BRAND VLBI signal chain. Therefore the sampler and BRAND board require particular attention.

3.3 Firmware

The implementation of the Firmware for the four Kintex Ultrascale FPGAs is by far the largest part in the software development process for the BRAND project, and is still ongoing. Progress has been delayed due to the late delivery of the hardware which is urgently needed for testing the firmware.

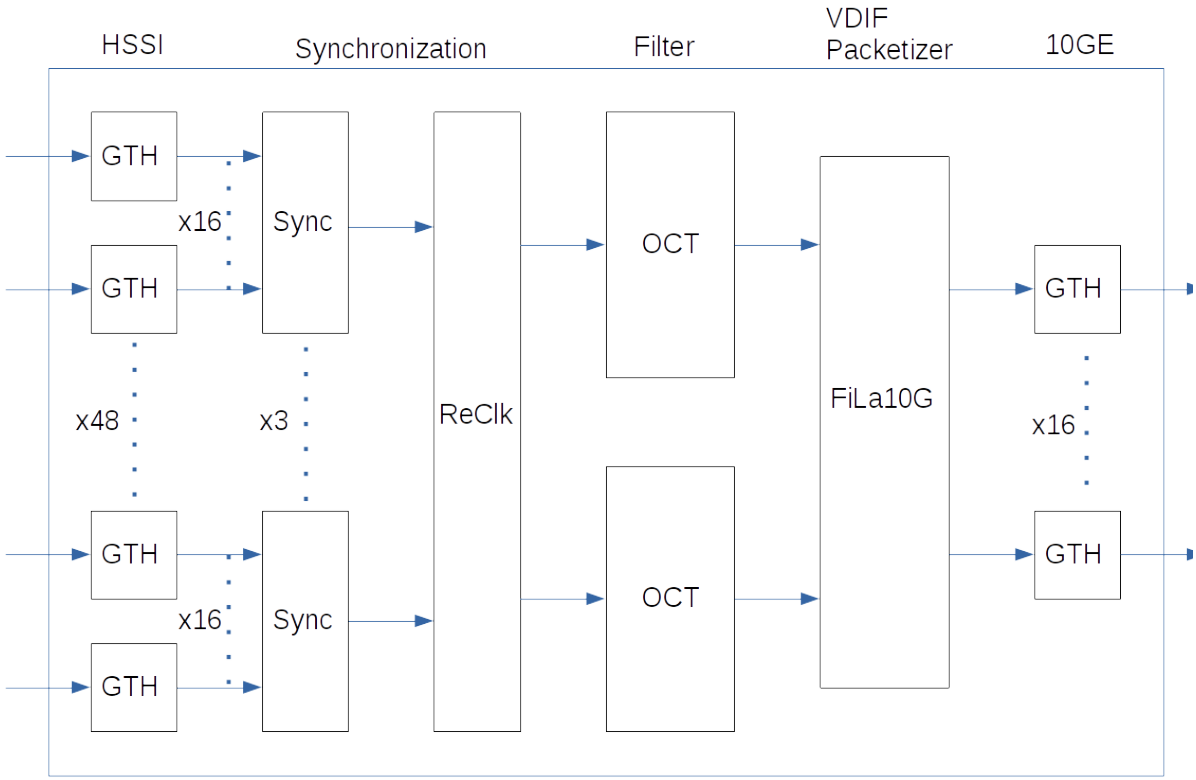

Figure 10: Block diagram of the software and signal flow in the Kintex FPGAs.

The Kintex FPGAs will receive the sampled data from the ADC at data rates of 2 x 28 GSps or 1 x 56 GSps at 8 bit for each FPGA. The band is then filtered with programmable parallel FIR bandpass filters to produce smaller bands. These bands are then sent to a packetizer unit which adds a timestamp, puts the data into VDIF formatted frames and sends them out to the next post processing unit, either a DBBC3 digital backend or directly to a recorder. The latter will be mostly used for debugging. To ease debugging of the BRAND_C board it was also decided to generate VDIF formatted data already at this stage. For analysing the data standard software can then be used.

The data transmission between sampler and FPGAs is performed using the HSSI (High Speed Serial Interface) protocol. Each FPGA has 64 GTH Transceivers[6] for this purpose. 48 are used

[6]Kintex UltraScale transceivers, type: GTH with peak 16.3 Gb/s for each of 64 transceivers. Total bidirectional data rate 2,086Gb/s.

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for the HSSI connection to the sampler, 16 are used as 10G Ethernet transceivers to send out the data.

This data transmission is the main part, which is still being worked on. This is done in cooperation with the sampler manufacturer, due to their experience with the HSSI interface. Work on this part could only be continued since the hardware became available.

The sampled data arrives at the FPGA with a data width of 3 x 128 Bytes per clock cycle, at a clock rate of 149 MHz. For the following processing stages the data rate is changed to 2x128 Bytes per clock cycle at a clock rate of 224 MHz. This data rate conversion unit is already implemented and tested in simulation.

The next processing stage is the filtering of the data, to limit the bandwidth to a size that can be managed and can be sent out to the final processing unit DBBC3. The filtering is done by OCT modules, which are programmable parallel FIR filters that are already in use in the DBBC3, as for example for EHT observations. These filters were modified to work with the available bandwidth, they are implemented and tested in simulation.

The filtered data is then processed in the next stage, which is the packetizing unit. This unit is based on the so-called FiLa10G part of the DBBC3 firmware which has already been in use in the field for a long time. The FiLa10G firmware was extended to work with the increased bandwidth and more outputs. The DBBC3 has four 10G Ethernet transceivers available to send out the data, each Kintex FPGA has 16 10G Ethernet transceivers available for this purpose.

The only parts of the DBBC3 firmware that cannot be used are the IP Cores for the Ethernet Transceivers. The DBBC3 uses Virtex 7 FPGAs with GTX Transceivers, so the IP Cores used there are not compatible with the Kintex devices, and have to be reimplemented.

In summary large parts of the Kintex firmware have already been implemented and tested, partially in use in the DBBC3 digital backend. The main issues are the receiving part of the data transmission from the sampler device, and the sending part for the 10G Ethernet transmission to the DBBC3. It is expected that the remaining problems can be solved in the next few weeks.

4 DBBC3 Digital Backend

Given the limited resources of the BRAND project it was decided in the planning stage that the DBBC3 would be used as the digital backend to form standard VLBI sub-bands and VDIF data packets. The DBBC3 had been developed by the JRA DIVA of the previous RadioNet3 (FP7-Grant Agreement no. 283393). It has been continuously improved since the end of RadioNet3 and is now the most widely selected wide-band VLBI backend. It has been used at the radio telescopes Pico Veleta and APEX. It is being used for tests with data-rates up to 32 Gbps in the EVN. A number of geodetic VGOS stations employ the DBBC3 as VLBI backend.

The DBBC3 offers three different firmware versions for channelising the 4 GHz of bandwidth per IF input – DDC (digital downconverter), DSC (direct sampling conversion), and OCT. The digital downconverter firmware is a port of the DDC from the DBBC2, which is the main mode used in the EVN and elsewhere. The DBBC3 DDC firmware offers the selection of up to 16 BBCs (= base-band converters with upper and lower sidebands = 32 sub-bands) per IF input with a selectable bandwidth between 2 MHz and 128 MHz per sub-band. The DSC firmware (direct sampling) offers the full 4 GHz band. The latest firmware, OCT, offers arbitrary band selection within the 4 GHz input IF with the use of one or two digital FIR-filters per IF input. An OCT mode with 1 GHz wide sub-bands for VGOS has been extensively tested by Onsala and Hobart, including a successful fringe-test with the Kashima antenna in Japan. The EHT OCT mode uses a 2 GHz wide OCT derivative which allows to split the 4 GHz down-converted and sampled baseband into two 2 GHz

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pieces (0 GHz to 2 GHz and 2 GHz to 4 GHz). This OCT mode offers full compatibility with the R2DBE backends.

A Polyphase filter bank (PFB) is on the list for future improvements. It would produce many more channels, but it can be emulated with the DDC when tuned in steps of twice the sub-bandwidth.

Figure 11: DBBC3 front view

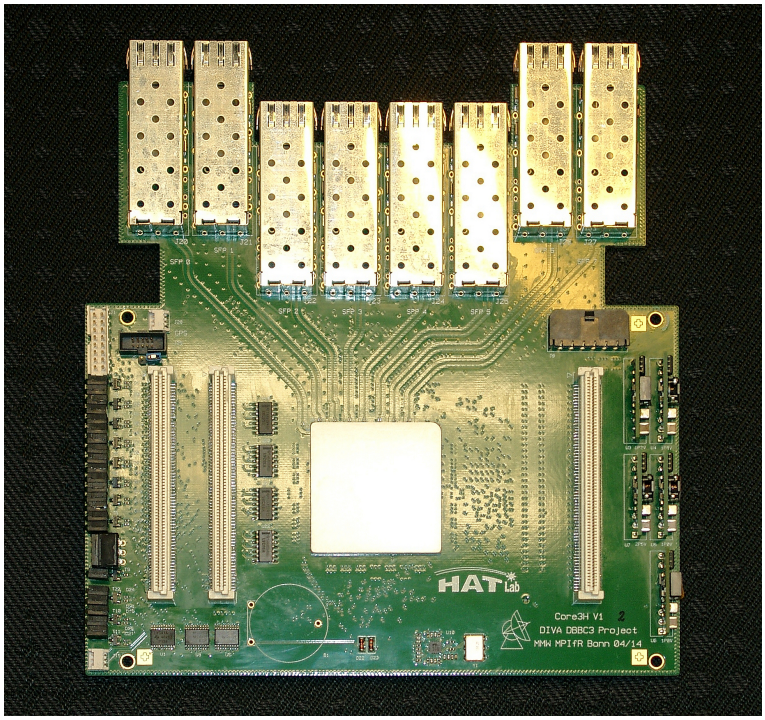

Figure 12: CORE3-H board. In the centre the FPGA can be seen. On the top are eight populated 10GE transceivers visible. The long connectors are the HSI, HSO, and command buses.

For T_{sys} measurement at EVN, VGOS, and elsewhere, the DBBC3 generates a TTL output signal at 80 Hz to switch the noise diode signal on and off for noise-adding radiometry and synchronously detects the total IF power in DDC firmware.

4.1 DBBC3 Hardware

The standard DBBC3 sampler board (ADB3L) uses four e2v sampler chips with interleaved sampling of 4 GHz wide bands. The digital data is sent to the processing board Core3H via the HSI[7] bus. This part of the DBBC3 as well as the analogue signal conditioning boards will not be used for the BRAND receiver.

On the Core3H board the data received is processed by a Virtex 7 485 FPGA. The processing functions are combined with multiple 10GE input/outputs ports. In the original DBBC3 the input ports are not used.

4.2 DBBC3 Firmware Changes

In its original form the DBBC3 consists of pairs of up to eight ADB3L ADCs and Core3H processing boards, which perform the digital processing of the data sampled by the internal ADCs.

[7] High Speed Input bus

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For the BRAND project the ADB3L ADCs will not be used, instead the Core3Hs will receive the data over the available 10G Ethernet lines. The currently available firmware does not have the capability to receive data over Ethernet, only the transmitting part is used. This was left out for performance reasons in the original RadioNet3 project.

The only other hardware change for the BRAND project is that the number of Ethernet transceivers has been increased from four to eight. In normal VLBI operation when data is only output via the transceivers a total of four is enough to handle all data passing through the Core3H processing boards.

The following firmware modifications are necessary for the BRAND project, and are currently implemented and tested:

- support for eight transceivers, instead of four.
- activation of the receiving part in the transceiver IP cores.
- synchronization of the incoming data to produce one parallel data stream

The synchronized data will then be processed by additional filters, either fixed bandpass filters (OCT mode) or variable Digital Down Conversion units (DDC mode). These modes are already implemented and are regularly used for observations with the DBBC3 digital backend.

4.2.1 Digital Polarisation conversion

The P.S.I. (Polarization State Indicator) system is the contribution of ASTRON to project BRAND.

Background theory:
An EM-wave is a transversal wave, consisting of electric field component E [V/m] and magnetic field component H [A/m], with the direction of propagation perpendicular to (E,H)-plane. Polarization refers to the electric field component E: this is a two-dimensional complex-numbered vector, with its x- and y-coordinates situated in the (x,y)-plane.
Depending on the phase-difference between Ex and Ey, the direction of vector E in the (x,y)-plane changes in time. This direction change is expressed via the polarisation state. The polarisation state can be linear (positive or negative 45 degrees slope), circular (right-handed or left-handed rotation), or elliptical

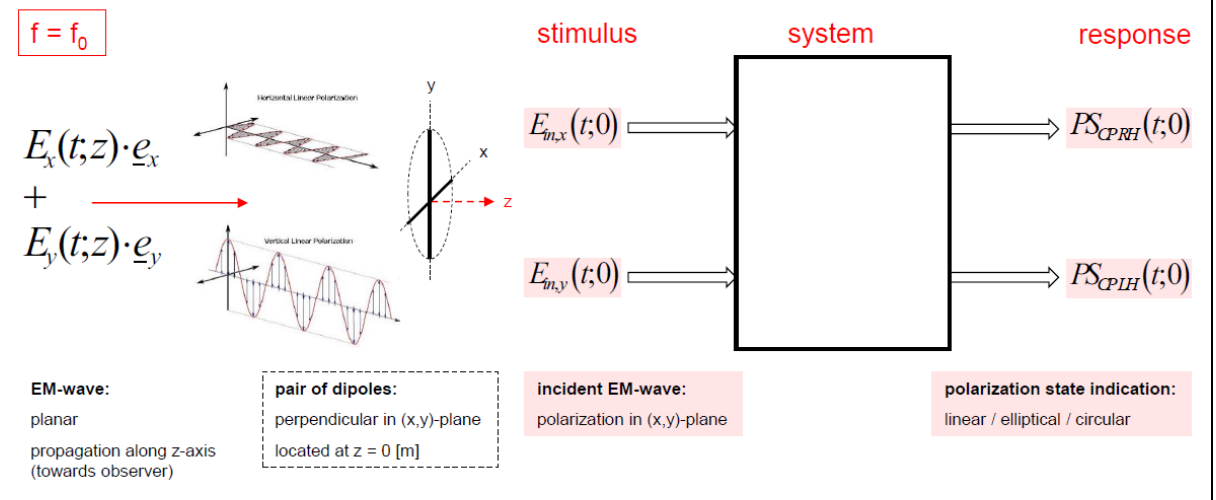

Figure 13: Polarisation State Indicator: functional context with its environment

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The Polarisation State Indicator (P.S.I.) extracts the polarization state of an incident EM-wave. This EM-wave originates from a crossed dipole-antenna pair, where the dipoles are directed along x-axis and y-axis respectively. Figure 13 shows a black-box model, which specifies the I/O-interface.

For single-tone ("extreme narrowband") processing, the incident electric field E(z;t) is a harmonic time-function.

The P.S.I translates the phase-difference between Ex and Ey into the polarization state of E.

The polarization state is captured by two signals (scalars), 'PS_CPRH' and 'PS_CPLH':

- if both signals are equal amplitude and same sign, then the polarization state is "linear, slope = +45°";
- if 'PS_CPLH' = 0 and 'PS_CPRH' ≠ 0, then the polarization state is "circular, right-handed";
- if both signals are equal amplitude and opposite sign, then the polarization state is "linear, slope = -45°";
- if 'PS_CPRH' = 0 and 'PS_CPLH' ≠ 0, then the polarization state is "circular, left-handed".

The relationship between input and output is specified by the table below.

$E_{in,x}(t;0) = E_0 \cdot e^{j\omega_0 t}$

$\Delta\varphi$	$E_{in,y}(t;0) =$	polarization state (x,y)-plane observed at z = 0	$\frac{PS_{CP\,RH}(t;0)}{E_0}$	$\frac{PS_{CP\,LH}(t;0)}{E_0}$
0	$E_0 \cdot e^{j\omega_0 t}$		$e^{j\omega_0 t} + e^{j(\omega_0 t + \frac{1}{2}\pi)}$	$e^{j(\omega_0 t + \frac{1}{2}\pi)} + e^{j\omega_0 t}$
$-\frac{1}{4}\pi$	$E_0 \cdot e^{j(\omega_0 t - \frac{1}{4}\pi)}$		$e^{j\omega_0 t} + e^{j(\omega_0 t + \frac{1}{4}\pi)}$	$e^{j(\omega_0 t + \frac{1}{2}\pi)} + e^{j(\omega_0 t - \frac{1}{4}\pi)}$
$-\frac{1}{2}\pi$	$E_0 \cdot e^{j(\omega_0 t - \frac{1}{2}\pi)}$		$e^{j\omega_0 t} + e^{j\omega_0 t}$	$e^{j(\omega_0 t + \frac{1}{2}\pi)} + e^{j(\omega_0 t - \frac{1}{2}\pi)}$
$-\frac{3}{4}\pi$	$E_0 \cdot e^{j(\omega_0 t - \frac{3}{4}\pi)}$		$e^{j\omega_0 t} + e^{j(\omega_0 t - \frac{1}{4}\pi)}$	$e^{j(\omega_0 t + \frac{1}{2}\pi)} + e^{j(\omega_0 t - \frac{3}{4}\pi)}$
$-\pi$	$E_0 \cdot e^{j(\omega_0 t - \pi)}$		$e^{j\omega_0 t} + e^{j(\omega_0 t - \frac{1}{2}\pi)}$	$e^{j(\omega_0 t + \frac{1}{2}\pi)} + e^{j(\omega_0 t - \pi)}$
$-\frac{5}{4}\pi$	$E_0 \cdot e^{j(\omega_0 t - \frac{5}{4}\pi)}$		$e^{j\omega_0 t} + e^{j(\omega_0 t - \frac{3}{4}\pi)}$	$e^{j(\omega_0 t + \frac{1}{2}\pi)} + e^{j(\omega_0 t - \frac{5}{4}\pi)}$
$-\frac{3}{2}\pi$	$E_0 \cdot e^{j(\omega_0 t - \frac{3}{2}\pi)}$		$e^{j\omega_0 t} + e^{j(\omega_0 t - \pi)}$	$e^{j(\omega_0 t + \frac{1}{2}\pi)} + e^{j(\omega_0 t - \frac{3}{2}\pi)}$
$-\frac{7}{4}\pi$	$E_0 \cdot e^{j(\omega_0 t - \frac{7}{4}\pi)}$		$e^{j\omega_0 t} + e^{j(\omega_0 t - \frac{5}{4}\pi)}$	$e^{j(\omega_0 t + \frac{1}{2}\pi)} + e^{j(\omega_0 t - \frac{7}{4}\pi)}$

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		input: incident EM-wave (z = 0)		output: polarization state (PS)	
(→ Lissajous diagrams)					
$\Delta\varphi$	polarization state (x,y)-plane observed at z = 0	$\mathrm{Re}\{E_{in,x}(t;0)\}=$ $=E_0\cdot\cos(\omega t)$	$\mathrm{Re}\{E_{in,y}(t;0)\}=$ $=E_0\cdot\cos(\omega t+\Delta\varphi)$	$\mathrm{Re}\{PS_{CPRH}(t;0)\}\overset{def}{=}PS_{CPRH,\mathrm{Re}}(t)=$ $=2\cdot E_0\cdot\cos(\omega t+\frac{1}{2}\cdot\Delta\varphi+\frac{1}{4}\pi)\cdot\cos(\frac{1}{2}\cdot\Delta\varphi+\frac{1}{4}\pi)$	$\mathrm{Re}\{PS_{CPLH}(t;0)\}\overset{def}{=}PS_{CPLH,\mathrm{Re}}(t)=$ $=2\cdot E_0\cdot\cos(\omega t+\frac{1}{2}\cdot\Delta\varphi+\frac{1}{4}\pi).\cos(\frac{1}{2}\cdot\Delta\varphi-\frac{1}{4}\pi)$
0			$E_0\cdot\cos(\omega t)$	$\sqrt{2}\cdot E_0\cdot\cos(\omega t+\frac{1}{4}\pi)$	$\sqrt{2}\cdot E_0\cdot\cos(\omega t+\frac{1}{4}\pi)$
$-\frac{1}{4}\pi$			$E_0\cdot\cos(\omega t-\frac{1}{4}\pi)$	$2\cdot E_0\cdot\sqrt{\frac{1}{2}+\frac{1}{4}\sqrt{2}}\cdot\cos(\omega t+\frac{1}{8}\pi)$	$2\cdot E_0\cdot\sqrt{\frac{1}{2}-\frac{1}{4}\sqrt{2}}\cdot\cos(\omega t+\frac{1}{8}\pi)$
$-\frac{1}{2}\pi$			$E_0\cdot\cos(\omega t-\frac{1}{2}\pi)$	$2\cdot E_0\cdot\cos(\omega t)$	0
$-\frac{3}{4}\pi$			$E_0\cdot\cos(\omega t-\frac{3}{4}\pi)$	$2\cdot E_0\cdot\sqrt{\frac{1}{2}+\frac{1}{4}\sqrt{2}}\cdot\cos(\omega t-\frac{1}{8}\pi)$	$-2\cdot E_0\cdot\sqrt{\frac{1}{2}-\frac{1}{4}\sqrt{2}}\cdot\cos(\omega t-\frac{1}{8}\pi)$
$-\pi$			$E_0\cdot\cos(\omega t-\pi)$	$\sqrt{2}\cdot E_0\cdot\cos(\omega t-\frac{1}{4}\pi)$	$-\sqrt{2}\cdot E_0\cdot\cos(\omega t-\frac{1}{4}\pi)$
$-\frac{5}{4}\pi$			$E_0\cdot\cos(\omega t-\frac{5}{4}\pi)$	$2\cdot E_0\cdot\sqrt{\frac{1}{2}-\frac{1}{4}\sqrt{2}}\cdot\cos(\omega t-\frac{3}{8}\pi)$	$-2\cdot E_0\cdot\sqrt{\frac{1}{2}+\frac{1}{4}\sqrt{2}}\cdot\cos(\omega t-\frac{7}{8}\pi)$
$-\frac{3}{2}\pi$			$E_0\cdot\cos(\omega t-\frac{3}{2}\pi)$	0	$-2\cdot E_0\cdot\sin(\omega t)$
$-\frac{7}{4}\pi$			$E_0\cdot\cos(\omega t-\frac{7}{4}\pi)$	$-2\cdot E_0\cdot\sqrt{\frac{1}{2}-\frac{1}{4}\sqrt{2}}\cdot\cos(\omega t-\frac{5}{8}\pi)$	$-2\cdot E_0\cdot\sqrt{\frac{1}{2}+\frac{1}{4}\sqrt{2}}\cdot\cos(\omega t-\frac{9}{8}\pi)$
				carrier amplitude	carrier amplitude

Table 1: I/O-relationship: phase-difference → polarisation state

For wideband processing, two options for realization of the P.S.I. exist:

- realization in frequency-domain: partitioning the RF-band into a multitude of narrowband channels, where each channel is suited for single-tone processing;
- realization in time-domain: processing of the entire RF-band all at once. In this case, we need a functional block that can achieve a 90 degrees phase-shift for all frequencies in the RF-band. Such a functional block is the Hilbert Transformer.

In the BRAND project, it has been decided to realize the P.S.I. in the time-domain.

4.2.1.1 Realization

The Hilbert Transformer is realised in the discrete time domain. The impulse response is truncated to M samples and shifted to non-negative time indices[8]. This results in the time-discrete Truncated Hilbert Transformer.

In the ideal case, the conceptual architecture consists only of two Truncated Hilbert Transformers and two Adders (see figure 14).

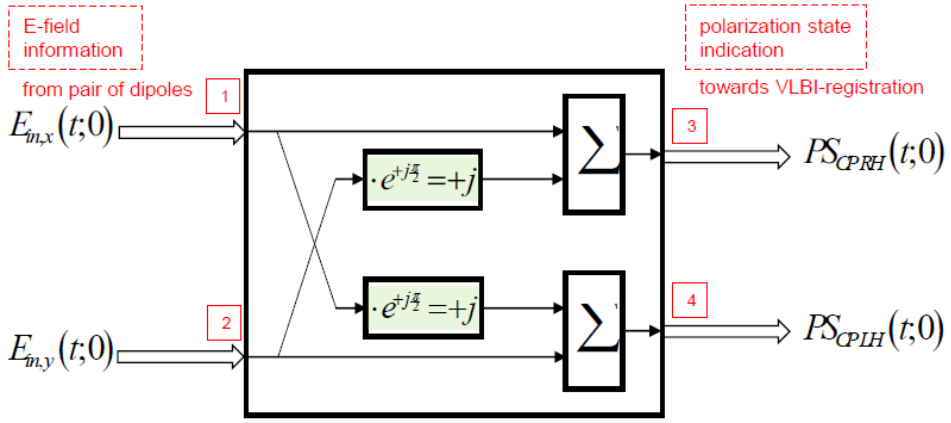

Figure 14: conceptual architecture – ideal case

[8] See also the more detailed document (Ref. 7) which will appear as ASTRON-report in 2-2021.

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In the realistic case, the dipole-antennas of the cross dipole-antenna pair are not exactly perpendicular and have different gains. Besides, they might have slightly different positions on the z-axis. See figure 15.

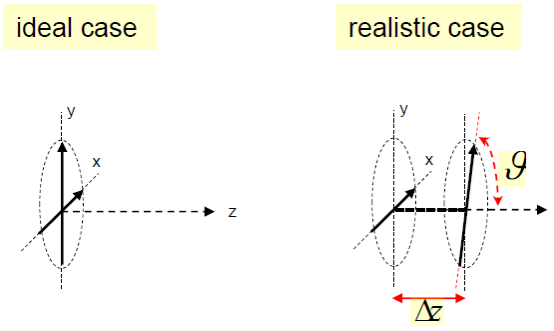

Figure 15: crossed dipole-antenna pair

In order to compensate for these deviations, two more functional blocks have been added for gain and phase calibration. See figure 16.

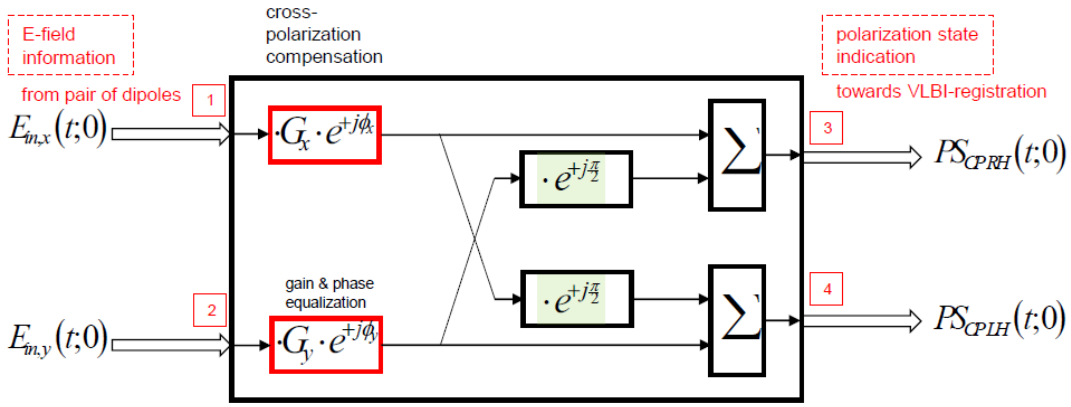

Figure 16: conceptual architecture – realistic case

Structure and behaviour of the P.S.I. model are specified in VHDL, an IEEE-standardized hardware description language [5]. Applying a structured top-down design methodology [6] leads to a detailed architecture, RTL (register transfer logic) coding style. See Figure 17.

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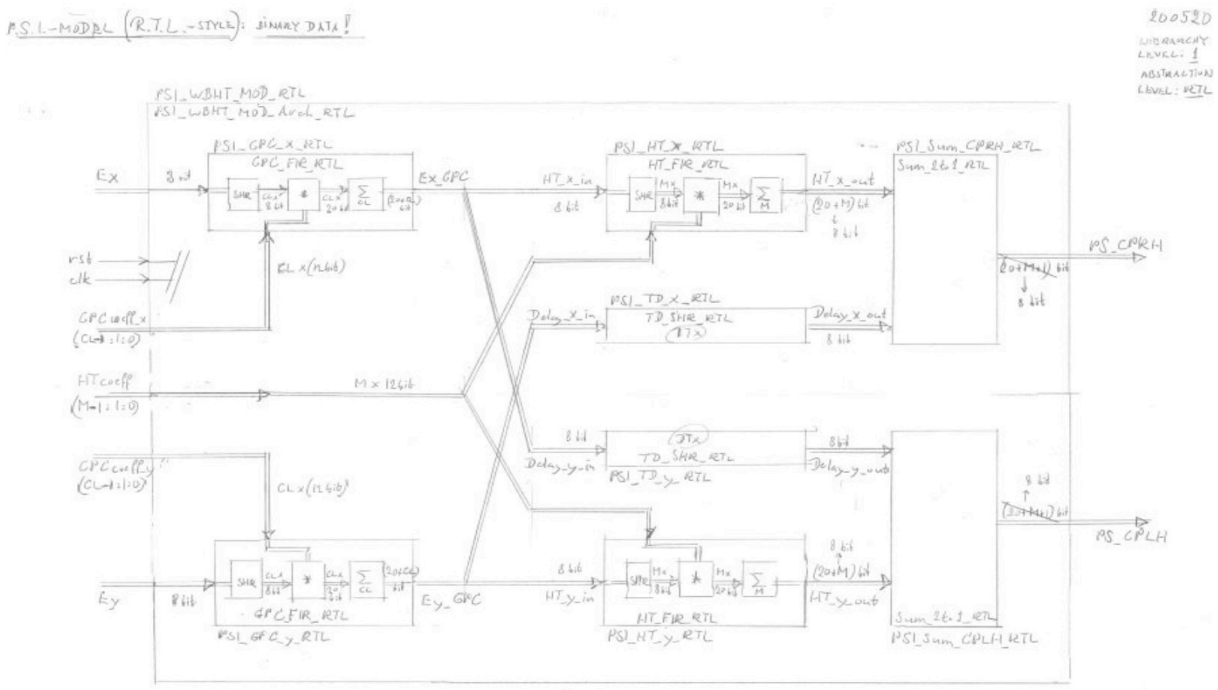

Figure 17: Detailed architecture (RTL level)

In the conceptual architecture, the addition of Ex and the 90-degrees phase-shifted version of Ey produces an incorrect result. Parallel to the Truncated Hilbert Transformer, a Delay Line is introduced that compensates for the group delay of the Truncated Hilbert Transformer. (The same holds for the addition of Ey and the 90-degrees phase-shifted version of Ex)

In the detailed architecture, signal processing is based on binary number (bit-vector) rather than real number format. As a consequence, the bit-vector at the output of the Truncated Hilbert Transformer has increased in size. In order to ensure that the Addition block operates on two input-terms with equal bit-vector size, the bit-vector at the output of the Delay Line is resized.

4.2.1.2 Simulation results

The stimulus generator of the test-environment inserts a sequence of 10 harmonic signals (with frequency points equally spaced between 0 and fs/2)[9] at the input, with for each frequency a sequence of 8 phase-differences (0 , 45 , 90 , … , 315 degrees).

At the output, we observe the waveforms shown in Figure 5, in particular the amplitudes of the indicator-pair ‘PS_CPRH’ and ‘PS_CPLH’:

- for phase-difference = 0 degrees, ‘PS_CPRH’ and ‘PS_CPLH’ have equal amplitudes, which indicates “linear polarization”;
- for phase-difference = 90 degrees, ‘PS_CPLH’ = 0 and ‘PS_CPRH’ has maximum amplitude, which indicates “circular polarization, right-handed rotation”;
- for phase-difference = 180 degrees, ‘PS_CPRH’ and ‘PS_CPLH’ have equal amplitudes, which indicates “linear polarization”;

[9] Fs = sampling frequency

- for phase-difference = 270 degrees, ‘PS_CPLH’ has maximum amplitude and ‘PS_CPRH’ = 0, which indicates “circular polarization, left-handed rotation”;
- for phase-differences = 45, 135, 225 and 315 degrees, ‘PS_CPRH’ and ‘PS_CPLH’ have unequal amplitudes (with ratios = 1 + √2), which indicates “elliptical polarization”.

The VHDL code of the P.S.I. model, after establishing the functional correctness, can be synthesized without problems to the FPGA technology of the Xilinx family.

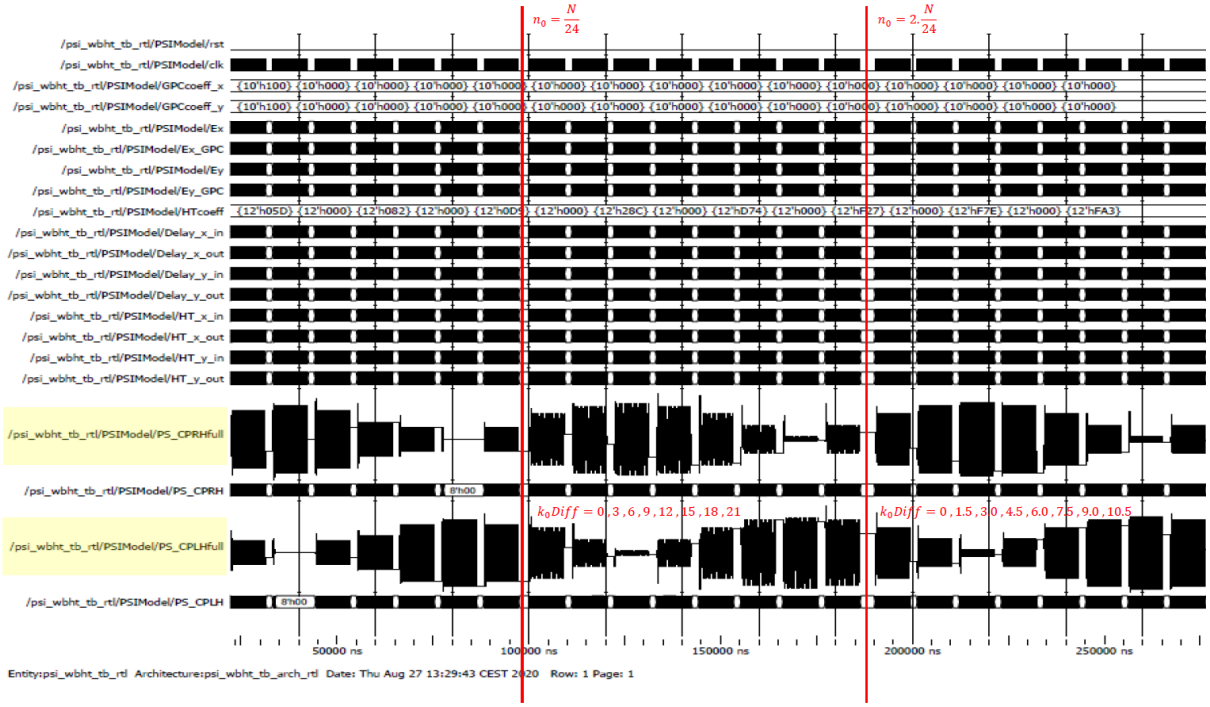

Figure 18: VHDL-simulation: waveform analysis – the first two of 10 sequences of harmonic signals; the 10 frequency points n0 are equally spaced on a spectral grid from 0 to fs/2 [Hz]

5 References

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6 Acronyms

10 GE 10 Gbit Ethernet
ADB3L DBBC3 sampler board

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ADC Analogue to Digital Converter
APEX Atacama Pathfinder Experiment (radio telescope)
ASIC application specific integrated circuit
BRAND BRoad-bAND
CORE3H FPGA processing board of the DBBC3
COVID-19 Corona Virus disease 2019
CP Circular polarisation with RH right hand and LH left hand
DBBC3 Digital Base-Band Converter 3rd generation
DDC Digital Down Conversion
DSC direct sampling conversion
DF Digital Frontend
e2v Company name
EHT Event Horizon Telecope
EM Electromagnetic with field components E and H
ENOB Effective Number of Bits
EVN European VLBI network
FFT Fast Fourier Transformation
FiLa10G Data packetising unit of the DBBC3
FIR Finite Impulse Response
FPGA Field Programmable Gate Array
FTDI Future Technology Devices Interglobal company
FX Refers to an FX correlator: Fourier transformation followed by cross correlation
GSps Giga samples per second
GTH Kintex UltraScale transceivers, type: GTH
GTX Virtex 7 FPGA transceivers
HSI / HSO DBBC3 bus
HSSI High Speed Serial Interconnect
ID Identifier
IF Intermediate Frequency
IP Internet Protocol
I/O or IO Input/output
OCT flexible in input band position and width filtering mode
PFB Polyphase filterbank
PSI Polarisation state indicator
RF Radio Frequency
RFI Radio Frequency Interference
RS232 Recommended Standard 232: Serial data protocol
SFP+ Small Form-factor Pluggable
SINAD power ratio between usefulsignal + noise + distortion and noise + distortion
T_{sys} System Temperature
TTL Transistor-transistor logic
USB Universal Serial Bus
VDIF VLBI Digital Interface Format
VGOS VLBI Global Observing System
VHDL IEEE-standardized hardware description language (FPGA programming)
VLBI Very Long Baseline Interferometry

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