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Multipixel W-band FPA demonstrator composed of cryogenic module and down conversion module

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	Some hardware described in this report comprises contributions from other members of the institutions participating in this work package.

Dissemination Level

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1 Introduction

The two goals of AETHRA WP5.1 “Semiconductor LNAs and MMIC receivers” were to investigate the new 35 nm gate length mHEMT technology available at IAF to improve noise performance of cryogenic MMIC LNAs at W-band (WP5.1.1) and to develop and build a W-band MMIC array demonstrator (WP5.1.2). Both goals have been successfully achieved, as described in this report. The MMIC chips were designed, fabricated and tested on wafer. Then, the MMIC chips were packaged and tested in modules, which were later assembled into a full W-band cryogenic array receiver demonstrator. The small FPA (Focal Plane Array) receiver demonstrator was validated in the laboratory. The instrument works very well, according to predictions, and can operate with state-of-the-art performance across the full 75-116 GHz band of design.

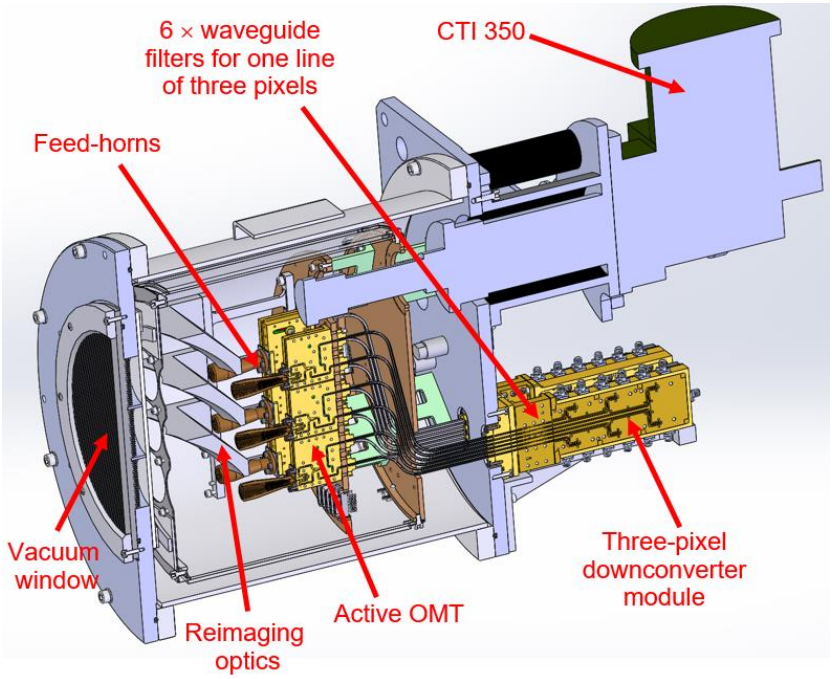

Fig. 1: *Cross-cut view of the dual-polarization nine-pixel cryogenic MMIC receiver array with room temperature sideband separating three-pixel downconverter modules. The reimaging optics and active OMT modules are cryogenically cooled at ≈15 K inside the cryostat by a commercial cryocooler (Cryodyne CTI 350).*

Fig. 1 shows a 3D image of the full 3×3 cryogenic receiver array we designed for AETHRA WP5.1.2. The optical design of the nine-element multibeam receiver is based on corrugated feed-horns and is optimized to provide an illumination edge taper Te=-13 dB of the IRAM 30-m Pico Veleta radio telescope sub-reflector. A feed spacing inside the cryostat of 44 mm provide a beam spacing on the sky of ≈1 arcmin, corresponding to ≈2.2 HPBW (Half Power Beam Width) at the 93 GHz central frequency. The fully reflective optics consists of two focusing mirrors at ≈300 K (not visible in Fig. 1) and of an array of individual optics maintained at ≈15 K that maximize the coupling between each feed-horn and the telescope. A large HDPE vacuum window (diameter ≈200 mm) consisting of 3×3 antireflection-coated sub-windows maintains a suitable low-level of vacuum pressure inside the cryostat, thus allowing to operate the cryogenic elements at the temperature of ≈15 K, as provided by a commercial cryocooler. A Goretex filter at 300K and a PTFE Infrared Filter at ≈70 K allow to strongly reduce the thermal loading on the cold stage. Two of the key modules of the receivers are the active OMTs (Orthomode Transducers), based on four W-band MMIC LNAs per module (two MMICs per polarization channel), and the three-pixel downconverter module (three three-pixel modules required for the nine-

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pixel elements). The active OMT modules have a small footprint, with size compatible with the 44 mm spacing between pixels. The downconversion scheme adopts dual-sideband separating mixers delivering two 4-12 GHz Intermediate Frequency (IF) output signals, the USB (Upper Sideband) and the LSB (Lower Side Band). A tuneable 14.50-17.33 GHz baseband LO (Local Oscillator) is injected into the downconverter, which is based on fully-integrated GaAs MMIC sub-harmonic mixers that include LO-multiplier and IF-LNA. The receiver is biased by a M&C (Monitor and Control) unit specifically developed for this project.

Only one row of the three-pixel lines of the nine-element array demonstrator of Fig. 1 was actually built and characterized in the laboratory. In particular, three active OMT modules and one three-pixel downconverter module were fully assembled, integrated into the FPA receiver demonstrator and tested in the laboratory.

2 Cryogenic pixel module

The cryogenic receiver pixel module is based on an “active” waveguide Orthomode Transducer (OMT) designed for dual-polarization radio astronomy observations across 75-116 GHz (3-mm band). The single-pixel receiver module consists of passive and active sections integrated in a single compact mechanical module as illustrated in Figure 2. The active OMT module adopts a square waveguide input (size 2.54×2.54 mm2) and two standard WR10 waveguide outputs (size 1.27×2.54 mm2) parallel to the input waveguide, as suitable for integration in a focal plane array.

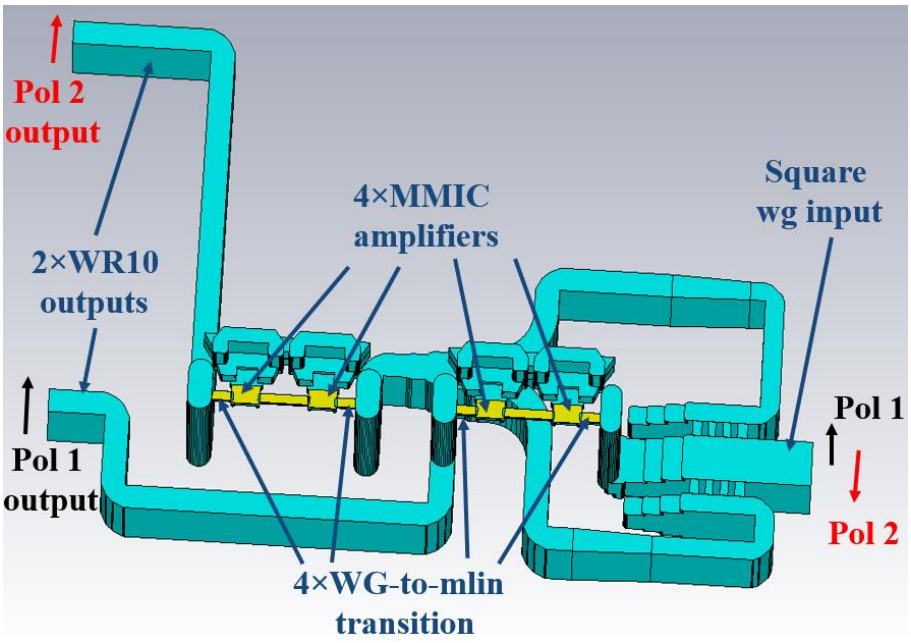

Fig. 2. *3D view of cryogenic single-pixel receiver module showing active (yellow) and passive parts (blue) of the module’s design.*

The passive section of the receiver module employs a broadband reverse-coupling waveguide OMT, while the active section consists of two ultra-low noise MMIC amplifiers in cascade, delivering a total gain of ≈45 dB for each of the polarization channels. The “active OMT” receiver is cryogenically cooled to a physical temperature of ≈15 K. The internal waveguide circuitry adopts oval waveguides for the injection and extraction of the signals into/from the MMIC LNAs through probe transitions on quartz

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substrate. Additional details on the design of the single-pixel module can be found in [1]. A planar OMT architecture was also considered for the module [2], but only the waveguide design of [1] was finally retained.

2.1 Design & fabrication of LNA MMICs

Each polarization of the active OMT contains two LNA MMICs in cascade. The first of which is optimized for lowest noise temperatures at cryogenic conditions. The second MMIC provides as well good noise performance; however, the design is optimized for a more favorable tradeoff between noise temperature, gain, and gain flatness. Both amplifiers are based on a noise-optimized 50-nm gate-length mHEMT technology of Fraunhofer IAF. A detailed comparison of the already-existing 50-nm and 35-nm mHEMT technology is given in deliverable 5.2 and in [1], [2]. As a result of this work, a noise-optimized version of the standard 50-nm mHEMT technology were developed. Details of the optimized 50-nm mHEMT technology are given in [3]

Each MMIC contains four stages in common-source configuration. Inductive source degeneration is used in all stages – in the first stage, for a more favorable simultaneously input noise and power matching and in the other stages, for an improved wideband performance. Further design details are given in [1].

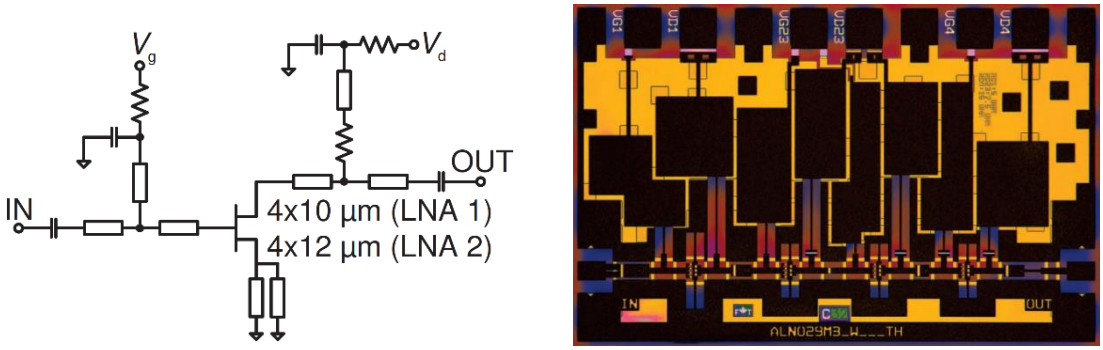

Fig. 3: *(Left) Simplified schematic of an amplifier stage. (Right) Chip photograph of a LNA MMIC. The dimensions of the chip is 1.5 mm x 1 mm [1].*

In Figure 4, the measured performance for different bias conditions of a waveguide test module is illustrated. The test module contains an LNA, which is used as the first MMIC in the active OMT. For a frequency range from 66-116 GHz and a bias current of 100 mA/mm, the measured average noise temperature is 29.1 K. It is important to mention that the losses of the vacuum window and the waveguide horn in front of the LNA are part of the measured performance.

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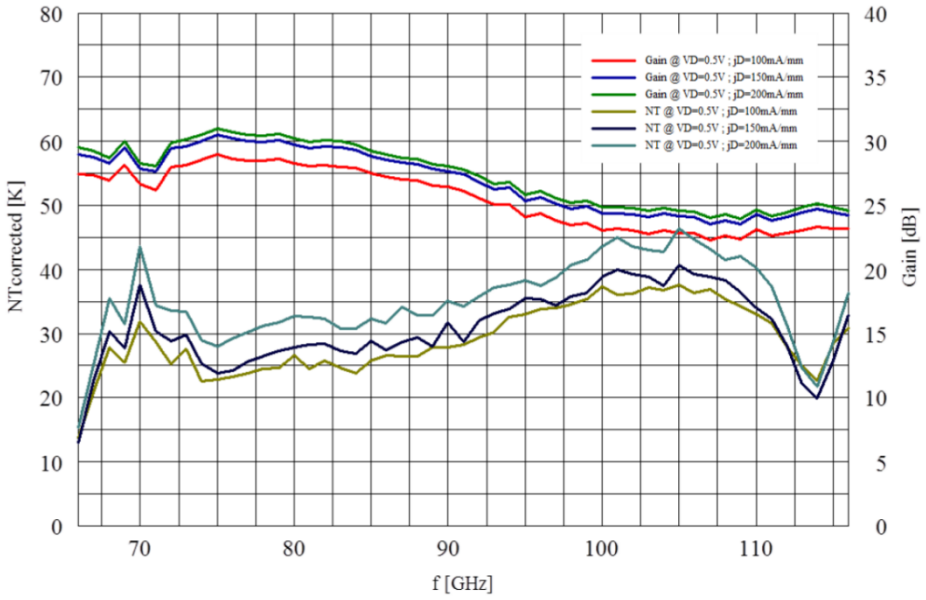

Fig. 4: *Measured noise temperature and gain at an ambient temperature of 13 K versus operating frequency for different bias conditions.*

2.2 Design of OMT

The OMT design is based on a symmetric reverse-coupling structure. The network representation of the passive section of the OMT, illustrating the principle of the symmetric reverse-coupling, is shown in Figure 5. Here, Pol 1 and Pol 2 propagate from a common input port (1). Pol 1 signal is fully coupled to the straight output port (4), while Pol 2 signal is equally split between two 90 hybrid couplers, whose output ports (5) and (6) are terminated with reactive loads (RL). Pol 2 signal is reverse-coupled (-3 dB coupling) to output ports (2) and (3) with a phase difference of 180 deg.

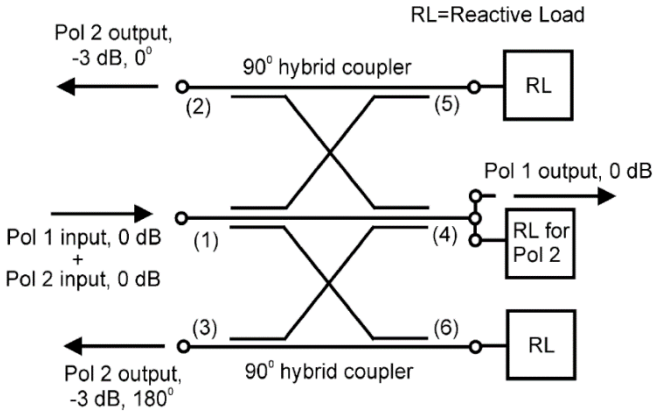

Fig. 5: *Schematic representation of the ideal polarization splitting network (OMT) with forward coupling of Pol 1 (from ports 1 to 4) and symmetric 3-dB backward coupling of Pol 2 (from port 1 to ports 2 and 3). The structure consists of two 90° hybrid couplers with reactively loaded (RL) outputs. Port 1 is in common to the two hybrids.*

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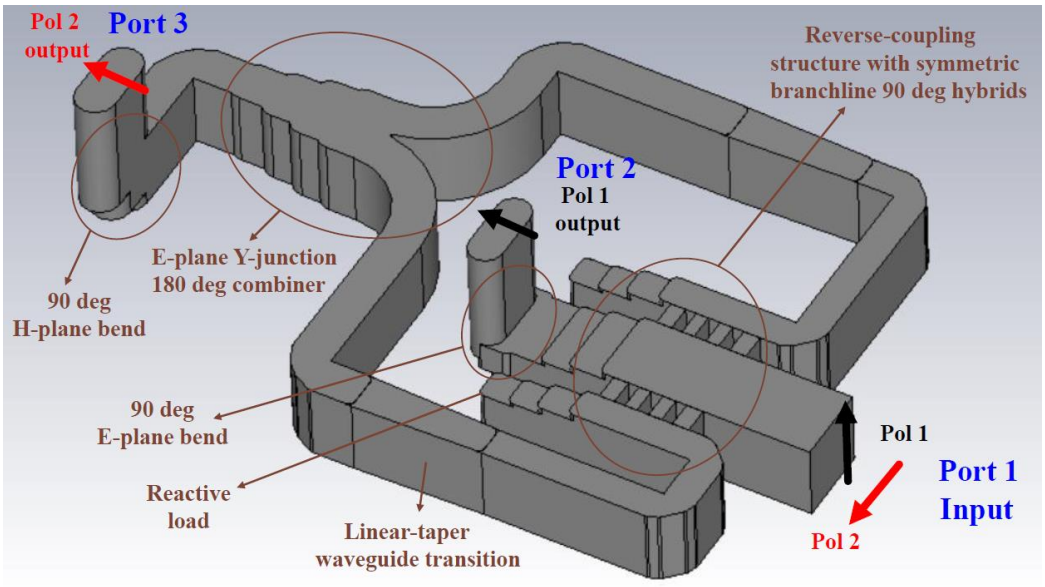

Fig. 6: *3D view of the internal waveguide circuitry of the OMT passive part, which includes the polarization splitting reverse-coupling structure with symmetric branchline couplers. Two orthogonal modes associated to Pol 1 and Pol 2 propagate from the input port (Port 1 on the right), which has square cross-section, and are extracted from independent single-mode outputs (Port2 and Port 3) with oval cross-sections.*

Figure 6 shows the design of the waveguide OMT passive part. Across the 75-116 GHz band of design, the square waveguide input (Port 1, with size 2.54×2.54 mm^2) propagates two orthogonal modes associated to Pol 1 and Pol 2. The OMT inner structure consists essentially of the dual-side backward coupler, of a 90 deg E-plane rectangular-to-oval waveguide bend transition for Pol 1, and of one E-plane Y-junction power combiner cascaded with a 90 deg H-plane bend for Pol 2. The output waveguides have oval cross-section and can be machined directly into the block with an end-mill; they have slightly different size and are inscribable in rectangles with dimensions 2.683×1.081 mm^2 (for Port 2), and 2.781×1.270 mm^2 (for Port 3). The electrical lengths of the two sidearms between the backward coupler outputs and the power combiner inputs must be identical to guarantee that the Pol 2 signals recombine with the proper phase. Two identical linearly tapered transitions between rectangular waveguides are used on the sidearms. The electrical length of the square waveguide input is minimized to reduce the cross-polarization that might be induced by possible mechanical misalignments between the two block halves of the passive part of the OMT. The full OMT was optimized using the commercial electromagnetic simulator CST Microwave Studio.

The results of the electromagnetic simulations of the OMT passive section of Figure 6 are illustrated in Figure 7. The input reflection coefficient is, respectively less than -18 dB for Pol 1 and -13 dB for Pol 2 across the 75-116 GHz band (Fig. 5, top panel). The transmission loss is, respectively greater than -0.1 dB for Pol 1 and -0.45 dB for Pol 2 (Fig. 5, bottom panel). The losses were estimated assuming the metal to be Gold with conductivity $\sigma_{Au}=4.561 \times 10^7$ S/m and include all the losses effects from the square waveguide input up to the two oval waveguide outputs. The predicted cross-polarization and isolation levels for the perfectly aligned structure shown in Fig. 4 are less than -60 dB across 75-116 GHz. A lateral misalignment between block halves of ±10 μm, due to mechanical tolerances, would result in cross-polarization and isolation levels of less than -30 dB

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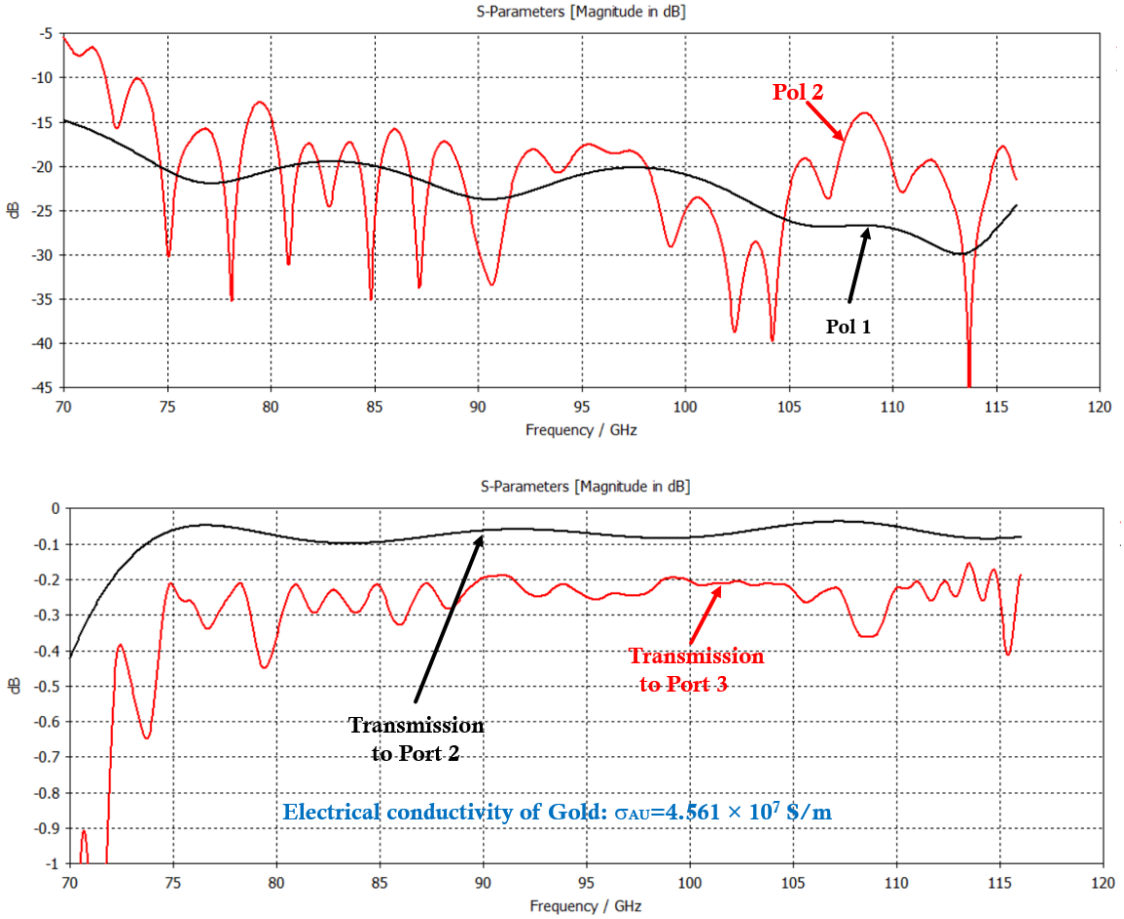

Fig. 7: *Electromagnetic simulation results of the passive section of the OMT shown in Fig. 5.*
Top: Reflection from square waveguide input. Bottom: OMT transmissions from square waveguide at port 1 to oval waveguides at ports 2 (Pol 1) and 3 (Pol 2).

2.3 Realisation & Tests

Primary goals for the design of the single pixel module were compactness and ease of fabrication at moderate cost. Thus OMT & LNAs were to be integrated in a single block and fabrication of the entire module should be feasible employing precision CNC-milling rather than more complicated and costly electroforming procedures. In addition, the possibility to do separate testing of OMT- and LNA-part of the single-pixel module has been considered to be highly desirable to allow for a modular design & debugging process.
Figure 8 shows a picture of the developed split-block design. The block consists of three parts, two of them containing the OMT with the module's square-WG input and two output waveguides. Also contained in the OMT-parts are four E- respectively H-plane stepped 90° bends that provide the vertical transition to the LNA- part of the block. These oval-waveguide transitions connect the OMT output waveguides to the LNA inputs and respectively, the LNA outputs to the outputs waveguides of the module. The third part contains two cascaded MMIC LNAs for each polarization and, for DC-bias supply and filtering, additional chip capacitors and a PCB with a micro-connector.
For separate testing of LNA and OMT parts two additional waveguide adapters were fabricated, one adapter providing direct access to the LNA waveguide inputs, the other adapter connecting directly to the OMT outputs. In particular, this allowed for separately testing the LNA-part even at cryogenic temperatures.

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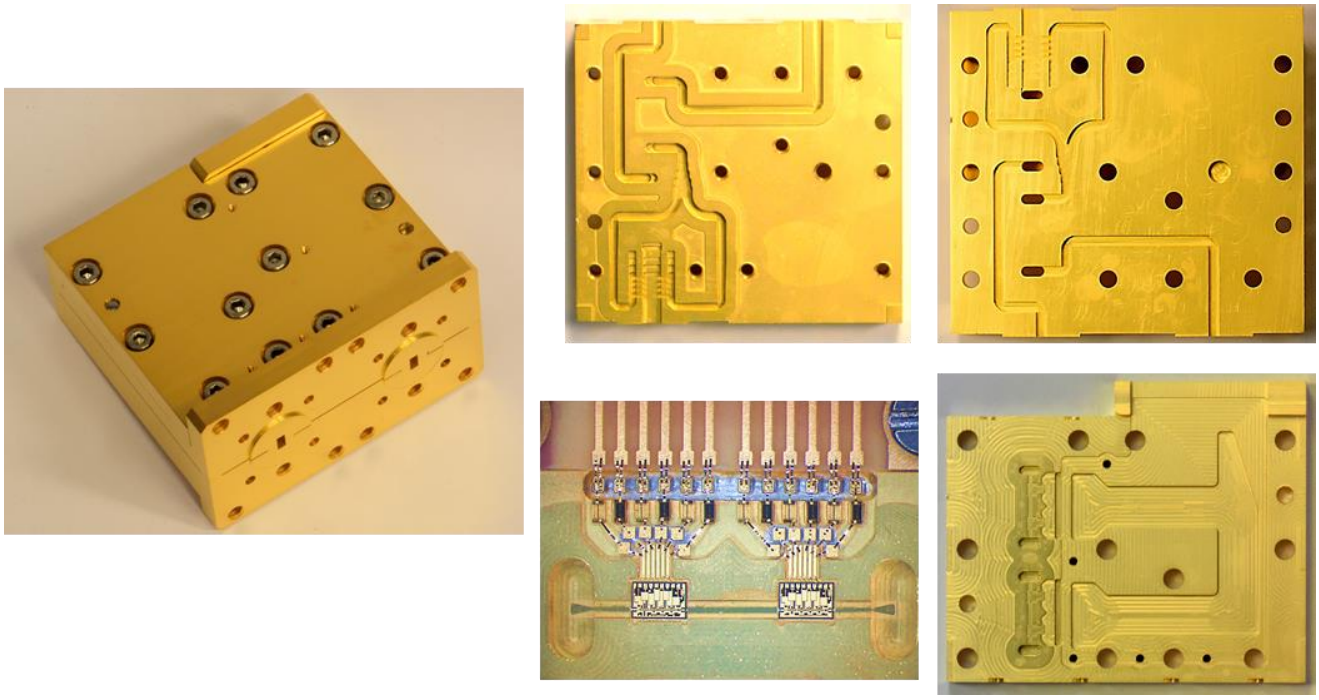

Fig. 8: *Left: Single-pixel module, assembly of three parts. External dimensions of the fully assembled active OMT are 43×25×35 mm^3. Top middle & right: OMT-parts with square-WG input, two WG outputs and milled 90° bends. Bottom right: LNA-part with one gain stage for each polarization. Bottom middle: Close-up of fully assembled single polarization gain stage showing wave-guide to microstrip transitions with backshorts, two cascaded LNA chips and components for DC-bias.*

In total, three of these single pixel modules SN#1-3 were assembled and tested for the demonstrator array, Figure 9 shows the LNA-parts of the three modules.

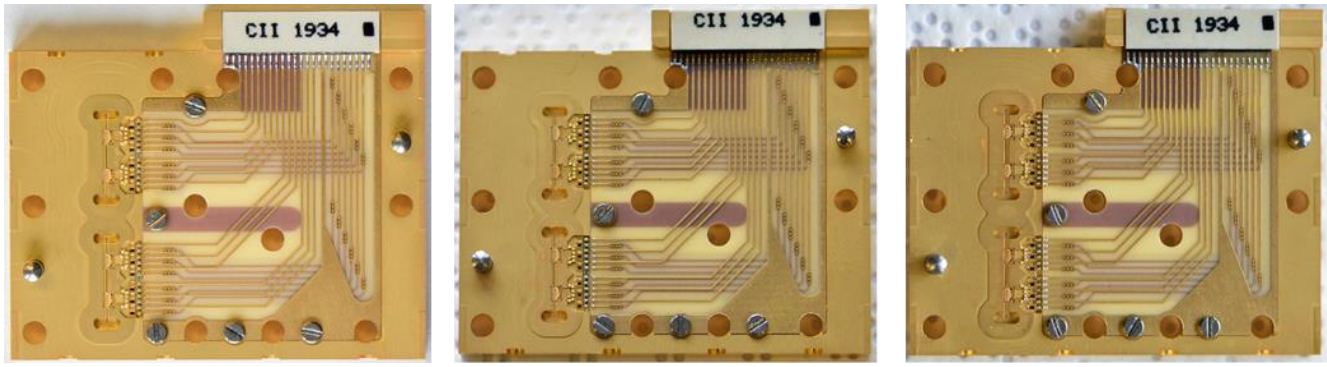

Fig. 9: *Assembled LNA-parts of the three single-pixel modules produced. Left to right: SN#1,2 & 3.*

Prior to sending modules for final integration into the demonstrator-array cryostat, several tests were carried out.
In detail, separate testing of the OMT part of module SN#1 was done at room temperature using the OMT-adapter. Test equipment used was a Keysight PNA-X vector network analyser equipped with two VDI W-band waveguide extender modules, covering 67-116GHz. For testing of the OMT two rectangular-to-square waveguide adapters were fabricated and verified. Results of the OMT tests are shown in Figure 10.1 and 10.2. As can be seen, the rectangular-to-square adapter needed for testing delivers good match and isolation and the OMT's performance closely follows the design simulations presented in section 2.2. It performs very well in the design frequency range of 75-116GHz, below ~74GHz insertion loss and match degrade, in particular for the sidearm coupled polarization (Pol2).

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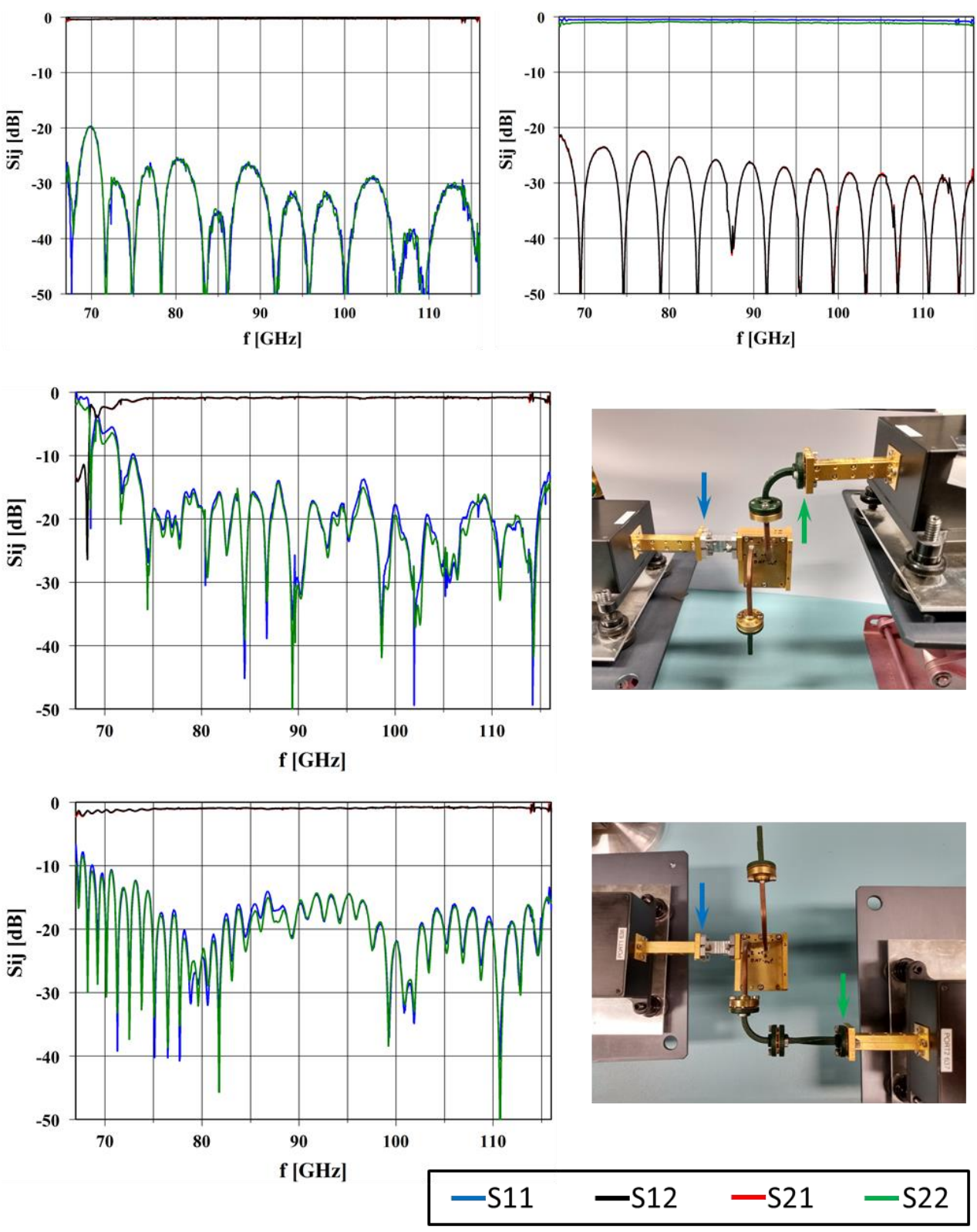

Fig 10.1: *Characterization of OMT-part of module SN#1 with OMT test-adapter. Top: Rectangular to square adapter, left: back to back, right: crossed polarizations. Middle: Square input Pol2 vs RWG output Pol2. Bottom: Square input Pol1 vs RWG output Pol1. Arrows in pictures denote calibration planes of port1 (blue) and port2 (green).*

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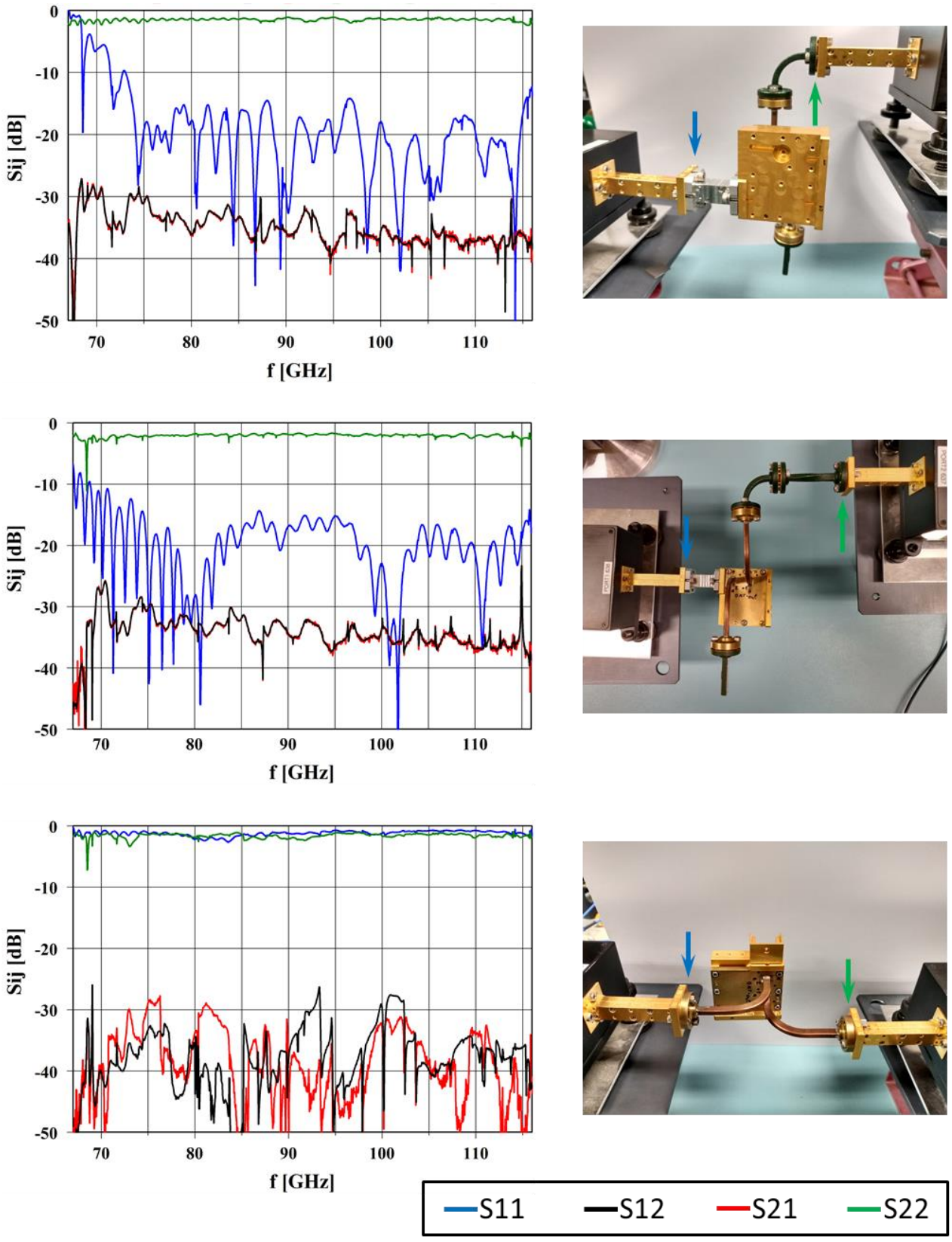

Fig 10.2: *Characterization of OMT-part of module SN#1. Top: Square input Pol2 vs RWG output Pol1. Middle: Square input Pol1 vs RWG output Pol2. Bottom: Cross-polarization isolation at RWG outputs with sqare waveguide shorted. Arrows in pictures denote calibration planes of port1 (blue) and port2 (green).*

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The tiny resonances appearing in all measurements at ~114 and ~116GHz are NOT caused by the OMT itself, but rather are present in the calibration already, thus probably being caused by using an extended frequency range above standard W-band. It has to be pointed out that these OMT measurements are not appropriate to determine an absolute value of insertion loss from square waveguide input to rectangular waveguide outputs of the OMT. From Figures 10.1 and 10.2 it's obvious that for mechanical reasons various components (bend, twist, adapter) are needed to measure both polarizations of the OMT. Due to the non-standard waveguide interfaces of some of these, a full de-embedding of the measurement is not feasible. However, later comparison of noise temperatures of the modules with and without OMT reveals, that losses can be in the range of few tenths of a dB only.

Next the LNA-parts of the single pixel modules were characterized at room-temperature using the PNA-X VNA plus W-band extenders. Since the minimum settable output power at the extender's waveguide ports is ~ -30dBm and the total gain of the two cascaded LNA's amounts to about 55dB in maximum, characterization of the LNA modules using the VNA is not straightforward. An input power of -30dBm would result in ~ +25dBm at the output of the second LNA – which is far above output saturation of the MMIC. In addition, calibrating at this low power levels would result in large trace noise. Solution was to include a precision attenuator at the input of the modules. Using the VNA, it was set to 35dB of attenuation, flatness of attenuation (+/- 0.5dB) and good input/output return loss (< -20dB) were verified. Thus in the results for modules SN#1-3, shown in Figure 11, 35dB have to be added to S21 and the measured S11 only represents the well matched precision attenuator. So in order to measure the (true) S11 of the module, we made an extra 1-port calibration of the VNA at lowest power level that still gave acceptable trace noise. Then, using the LNA-adapter, S11 of module SN#3 was measured without attenuator and leaving the 2nd MMIC unbiased to avoid saturation effects. Results are displayed in Figure 11 (bottom right).

Comparing left (LNAs + OMT) and right column (LNAs + test-adapter), Pol2 shows some gain ripples below ~74GHz. This is due to the performance roll-off in the sidearm coupled channel of the OMT (Pol2) that was already seen in the OMT measurements (Figure 10.1).

Noise temperature characterization of the modules at room temperature and 15K was done next, results are shown in Fig. 12. Measured noise temperatures of the modules are below 50K over the full band from 67-116GHz, clearly confirming the very good noise performance of the single chip previously shown in Fig.4. Again, these noise temperature measurements were done using absorber loads at room- and liquid nitrogen temperatures and NO correction has been applied for horn- or window losses. Due to the high gain (> 40dB) of the module, contribution of 2nd stage noise is below 1K, so NO correction for that was applied either.
Also, losses of the OMT seem to have negligible influence on noise performance at cryogenic temperatures as can be seen from comparing noise temperatures measured with the LNA adapter to noise temperatures of the full module with OMT (Figure 12). In contrast to that, differences between adapter- and OMT-measurements seem to turn up at room temperature at least for SN#3 in Figure 12, but so far no congruent picture reveals from the measurements of only three modules.

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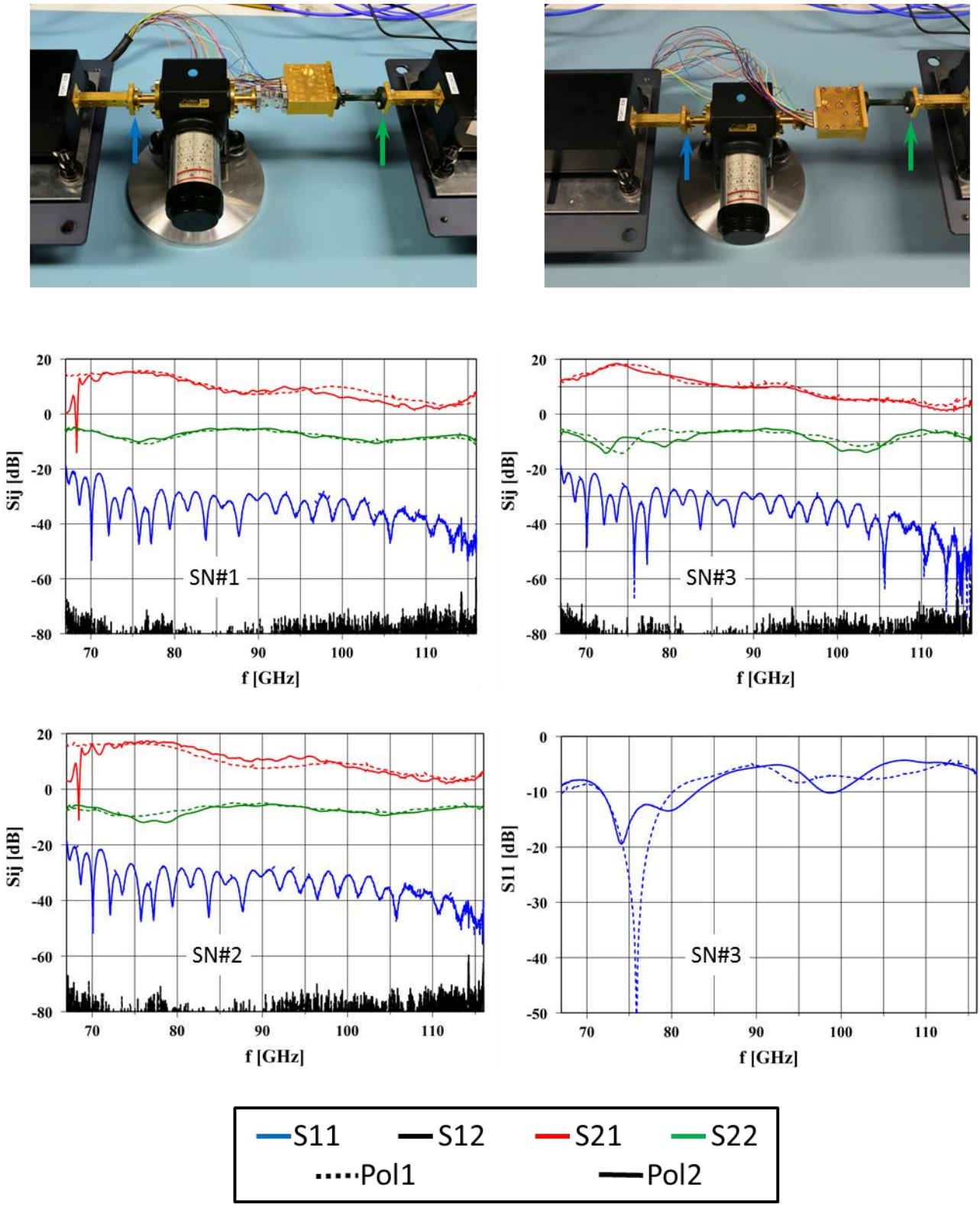

Fig 11: *Characterization of single-pixel modules at room temperature with VNA. Left column: LNAs with OMTs. Top: Photo of setup. Middle: SN#1. Bottom: SN#2. Right column: LNAs with test-adapter. Top: Photo of setup. Middle: SN#3. Bottom: SN#3, (true-) S11 measured without 35dB attenuator, 2nd MMIC unbiased (see text). Arrows in pictures denote calibration planes of port1 (blue) and port2 (green).*

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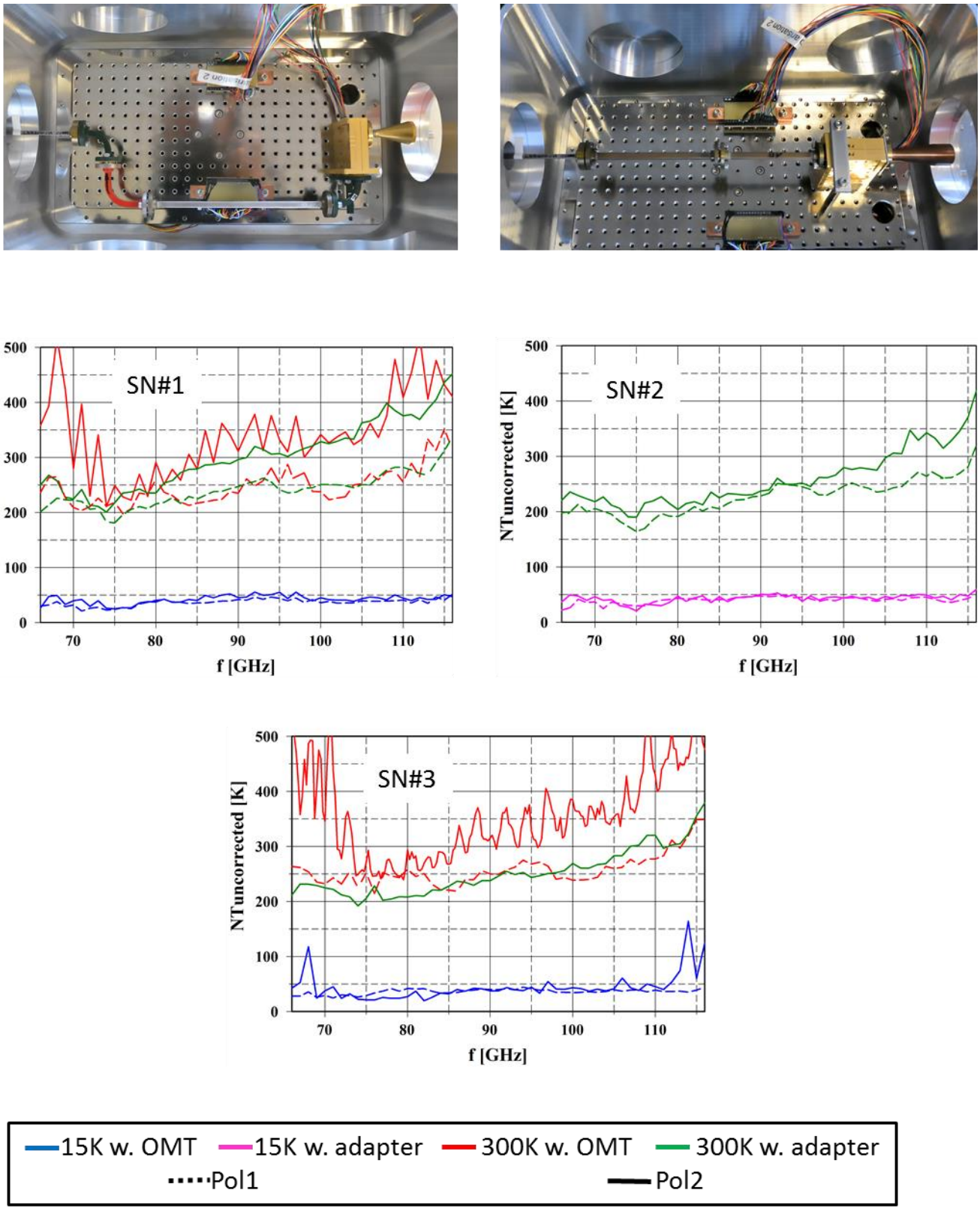

Fig 12: *Noise temperature of single-pixel modules at 300K and 15K.*
Top row: Test cryostat with modules. Left: Module tested with LNA test-adapter. Right: Module tested with OMT. Middle and bottom row: Test results of modules SN#1-3

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3 Fully integrated W-Band Downconverter

3.1 Design & fabrication of Downconverter MMIC

The fully-integrated down-conversion MMIC has the following requirements. Firstly, the baseline frequency ranges are (goal values are given in brackets): RF 75-116 GHz (72-116 GHz) and IF 4-12 GHz (3-13 GHz). Secondly, the MMIC aims to be pumped by a frequency-tunable LO tone in the approx. 14-18 GHz range (to be discussed further down). The LO steps within the LO frequency range to cover the entire RF range with the given IF bandwidth. Thirdly, the down-conversion MMIC should enable a receiver with a sideband-separating approach. Thus, an I/Q-mixer topology is required. Fourthly, to avoid interference issues of the LO signal at the IF outputs, the LO input frequencies should be outside the IF range which means above 13 GHz, but should be below 20 GHz. Therefore, a multiplication factor of the LO frequencies of six is needed. This can be realized, e.g., by an LO chain with a multiplication factor of six or by an x3 in combination with a subharmonically-pumped mixer. In this project, the latter of which was chosen. Compared to a frequency multiplier by six (x6), an x3 is easier to realize in a fully-integrated down-conversion MMIC. This is, due to filtering reasons, especially the case when targeting fairly wideband multipliers. Furthermore, an x6 would require either a direct multiplication by six which is, in general, considerably inefficient, or two multiplication stages which increases the occupied chip area and makes the filtering and avoidance of spurs even more challenging. A block diagram of the presented fully-integrated down-conversion MMIC is illustrated in Figure 13. To obtain a maximum of isolation between the individual building blocks while still achieving a considerably compact layout, each sub-circuit is designed in a grounded-coplanar waveguide environment.

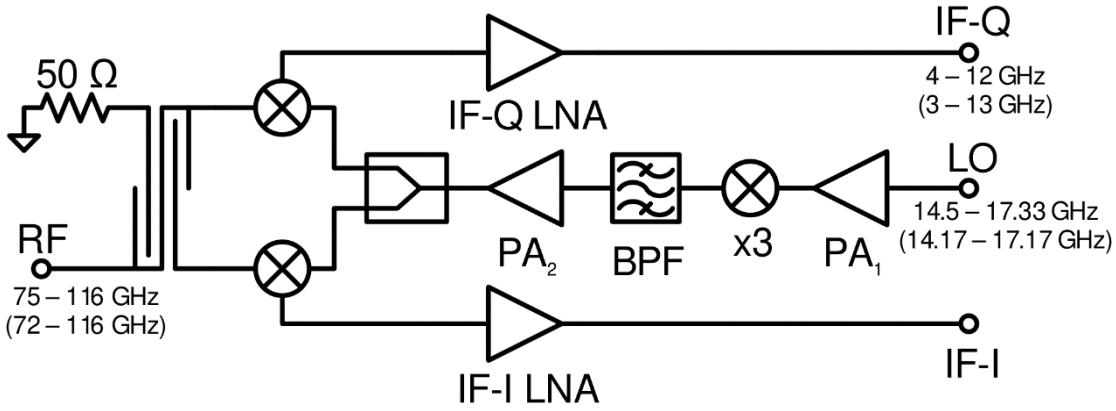

Fig. 13: *Block diagram of the presented fully-integrated down-conversion MMIC. The baseline frequency ranges are depicted at the corresponding ports. In addition, the frequency goals are given in brackets.*

The mixer cells and the x3 are based on an anti-parallel Schottky diode topology. The diodes feature a Schottky contact with a size of 0.25x4 µm² each and use the same process flow so that diodes and HEMT are simultaneously available. Each nonlinear circuit utilizes eight diodes. The mixer cell contains dedicated filter networks at all ports to improve the isolation of the ports to each other. Based on measurements of a test structure, the single-sideband conversion gain (CG_{SSB}) of the mixer cell is about -12 to -11 dB while covering at least the W-band frequency range with an IF of at least 0-15 GHz. At the RF input of the fully-integrated MMIC, a Lange coupler is used as 3-dB quadrature coupler. From 66-118 GHz, the coupler exhibits a measured amplitude and phase imbalance of less than ±0.5 dB and ±1°, respectively. Measurements of an I/Q-mixer test structure, including a Lange coupler, two mixer cells, and a Wilkinson splitter, demonstrate a CG_{SSB} in the range of -16 to -14 dB, which corresponds to the expectations. Figure 14 depicts a chip photograph and the measured CG_{SSB} of the separately fabricated test I/Q-mixer MMIC.

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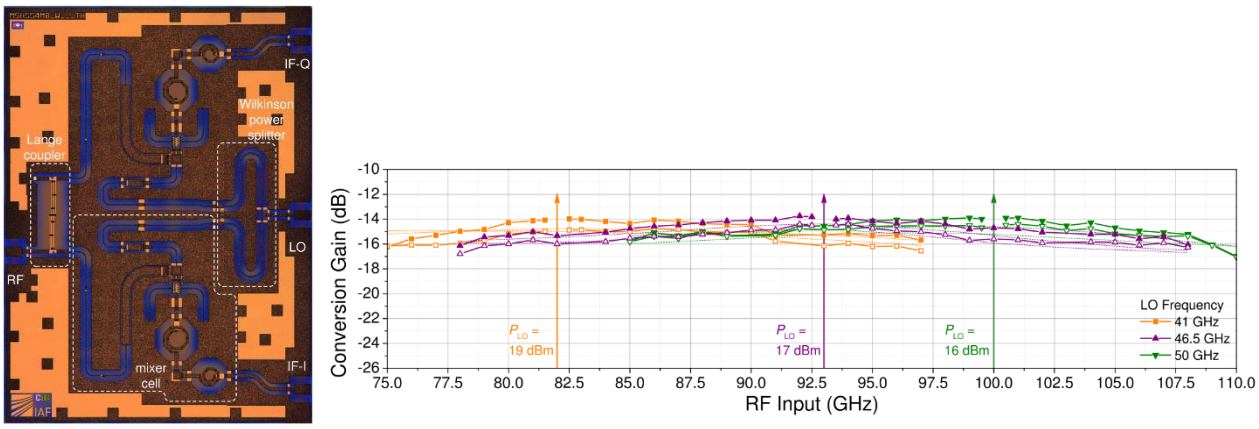

Fig. 14: *(Left) Chip photograph of the I/Q-mixer MMIC with a size of 1.5 mm × 2 mm. (Right) Measured conversion gain of LSB and USB versus RF input for three different LO frequencies. The arrows indicate the doubled LO frequencies. The RF input power is set to -20dBm and the conversion gain of the IF-I and IF-Q output is indicated by filled and open symbols, respectively.*

The central building block of the LO chain is the x3 which can be biased so that the output power can be adjusted between -8 and 0 dBm with almost constant conversion efficiency. Due to the anti-parallel diode topology, even harmonic frequencies can be expected to be well suppressed. Thus, the filtering of unwanted harmonics has to focus mainly on the fundamental and the fifth harmonic. Therefore, a band-pass filter is integrated after the x3 which lowers the fundamental by at least 30 dB and the fifth harmonic by approximately 5 dB. At the LO input, a PA (PA_1) is used to drive the x3. It is a two-stage amplifier with a 4x125 µm HEMT in the first stage and a 6x125 µm HEMT in the second stage. PA_1 can deliver an output power of 16 to 18 dBm while requiring an input power of up to 0 dBm. PA_2 amplifiers the output signal of the x3 and provides the LO drive power for the I/Q-mixer. PA_2 uses three stages with 4x65 µm HEMTs in the first two stages and a 8x80 µm HEMT in the output stage. With an input power of 0 dBm, the amplifier can deliver 16 to 17 dBm at the output. A chip photograph and the measured output power of the first to ninth harmonic of an integrated LO chain test MMIC is shown in Fig. 15 for a constant input power of -5 dBm. Further details about the sub-circuits are discussed in [4]. Each IF path comprises a two-stage LNA with a 4x35 µm HEMT per stage. To prevent issues with

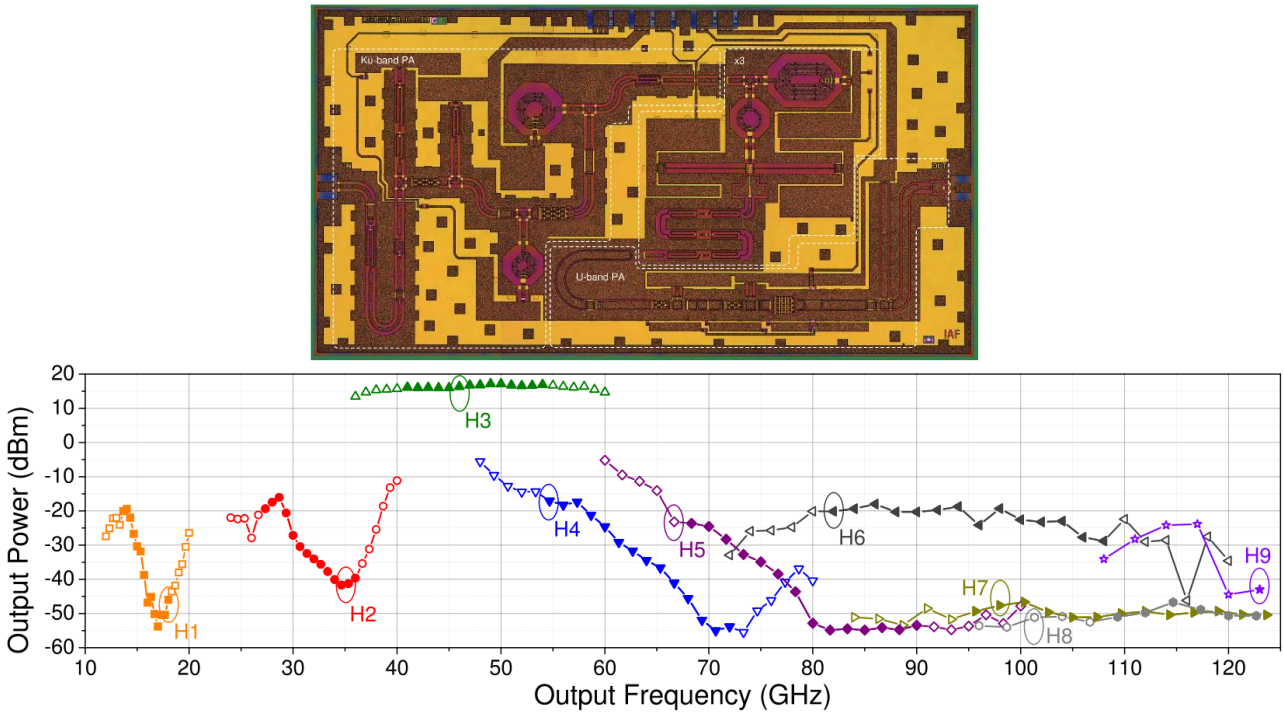

Fig. 15: *(Top) Chip photograph of the fabricated LO chain test MMIC. The chip size is 3.25 mm x 1.75 mm. (Bottom) Measured frequency response of the LO chain test MMIC for a constant input power of -5 dBm. The baseline frequency range (H3 frequency: 41-54 GHz) is indicated by filled symbols.*

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standing waves, specific attention was paid to the input and output return loss of the LNAs. Therefore, especially the first stage feature an inductive source degeneration to obtain good simultaneous input noise and power matching. The LNA is designed for a frequency range from 3-13 GHz. Based on simulations, a flat noise figure of below 1 dB is expected, which enables an overall flat noise performance of the entire down-conversion MMIC. The simulated gain of the LNA is 27-31 dB (with a falling slope towards higher frequencies).
In Figure 16, a photograph of the fabricated fully-integrated W-band down-conversion MMIC is depicted.

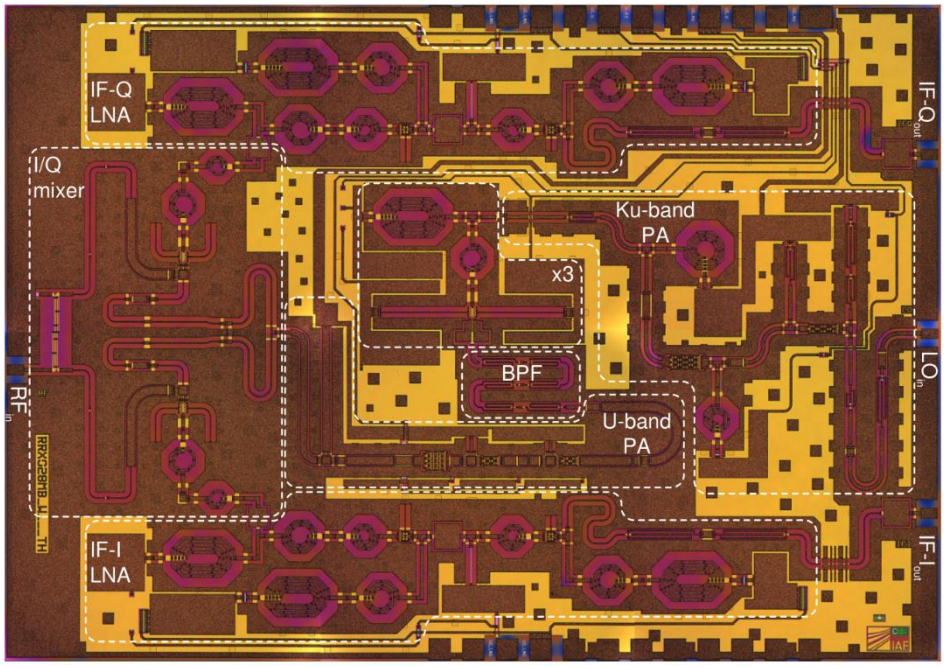

Fig. 16: *Photograph of the fabricated fully-integrated down-conversion MMIC. The chip has a size of 4.25 mm x 3 mm.*

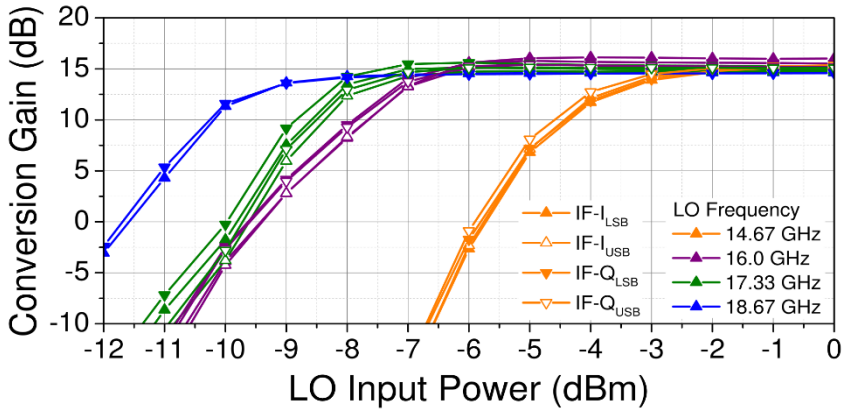

Fig. 17: *Measured CG_{SSB} as a function of LO input power for four different LO frequencies. The IF is 4 GHz. The RF input power is −25 dBm. LSB and USB are illustrated by closed and open symbols, respectively.*

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In Figure 17, CG_{SSB} is shown as a function of LO input power (P_{LO}) for LO frequencies of 14.67, 16, 17.33, and 18.67 GHz and for the lower sideband (LSB) and upper sideband (USB), respectively. For the higher LO frequencies, the conversion gain saturates for a power level of more than -5 dBm. For the lowest LO frequency, an LO input power of more than -1 dBm is required. In saturation, CG_{SSB} is for all measured combinations within 14.6-16 dB. For the same LO frequencies, the measured CG_{SSB} is shown as a function of RF in Figure 18. The MMIC exhibits a good conversion gain for the aimed IF range from 3 to 13 GHz with a difference between the sidebands and IF paths of less than 1 dB over most parts of the band. Even in extreme cases, the difference is below 1.7 dB. At the lower IF band edge, the conversion gain achieves values of 16-17 dB.

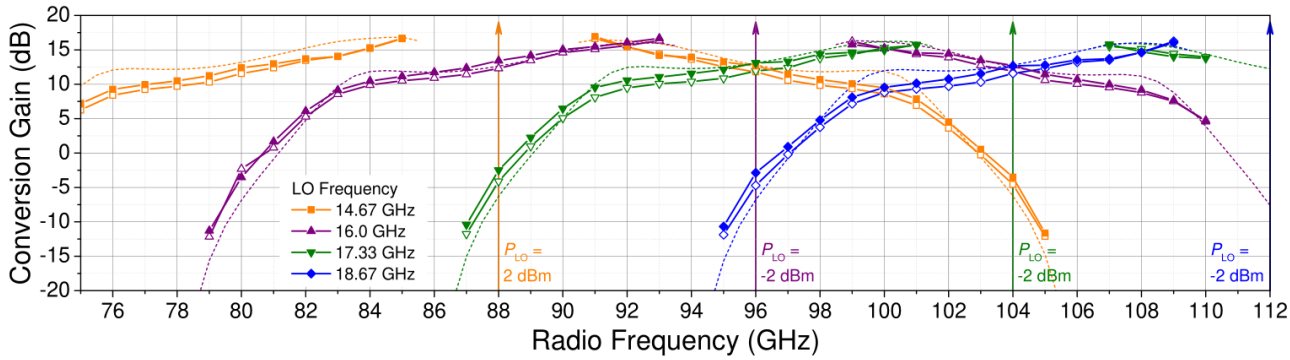

Fig. 18: *Measured (symbols) and simulated (dashed lines) single-sideband conversion gain as a function of radio frequency. CG_{SSB} of LSB and USB is measured for four different LO input frequencies and a fixed-LO scenario. The data for the I and Q path of the MMIC are given in closed and open symbols, respectively. As indication for the LO, arrows illustrate the sixfold LO input frequency. P_{LO} is given at the corresponding arrow. The RF input power is −25 dBm.*

The measured DSB noise figure is illustrated in Figure 19 as a function of IF for the corresponding RF range, which is determined by the calibrated frequency range of the noise source. The noise figure shows a flat performance for an IF from at least 3 to 13 GHz. The average DSB NF is between 14.2 and 15.4dB for all measured combinations.

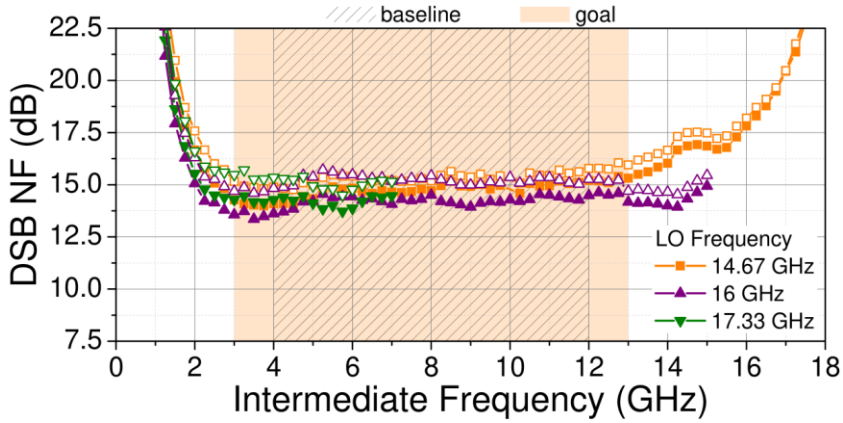

Fig. 19: *Measured double-sideband noise figure as a function of intermediate frequency for three LO frequencies in the W-band RF range. The LO input power is similar as in Figure 7. The data for the I and Q path of the MMIC are given in closed and open symbols, respectively*

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3.2 Block for single Downconverter MMIC, Tests

Prior to design and fabrication of a highly integrated downconverter module that would contain several chips, a single-MMIC downconverter test-block (Figure 20) was designed and fabricated. This was to carry out harmonic and sideband rejection tests, which are needed to validate the concept of the fully integrated MMIC downconverter chip, but could not be done during on-wafer testing of the chip due to lack of the IF-hybrid in the on-wafer test setup. The sideband separating MMIC downconverter chip integrates almost all components needed for a sideband separating mixing scheme: RF-hybrid, subharmonic mixers, LO power splitter, an LO-chain comprising of filter, 2 PA's and a tripler and 2 IF-amplifiers. Only the IF hybrid-coupler has to be added externally since the latter would be too big (costly) to integrate on-chip thus the on-chip IF-output are I&Q signals.
Figure 21 depicts the 4-12GHz 3dB 90° IF-hybrid that was designed and fabricated on 200µm fused-quartz substrate.

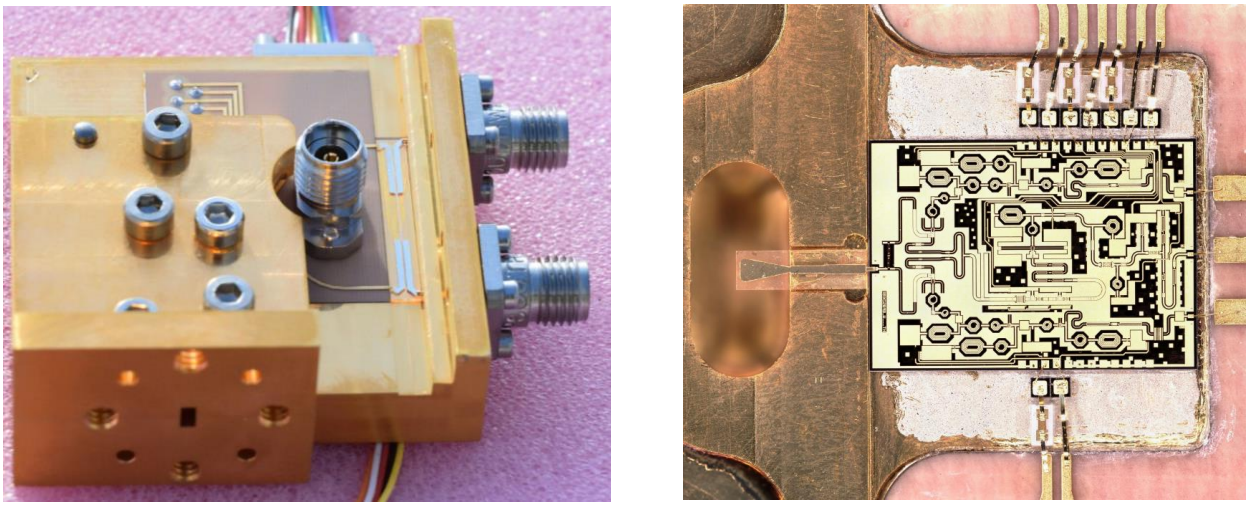

Fig. 20:. *Left: Single pixel downconverter module showing the WR10 waveguide input for the RF signal, the K-connector for baseband 14.5-17.33GHz Local Oscillator injection on top, the 4-12 GHz planar hybrid on quartz substrate, and the two coaxial outputs with LSB and USB 4-12 GHz IF signals.*
Right: fully-integrated MMIC downconverter packaged with E-field probe on quartz (left), LO-input and I/Q IF outputs in microstrip (right).

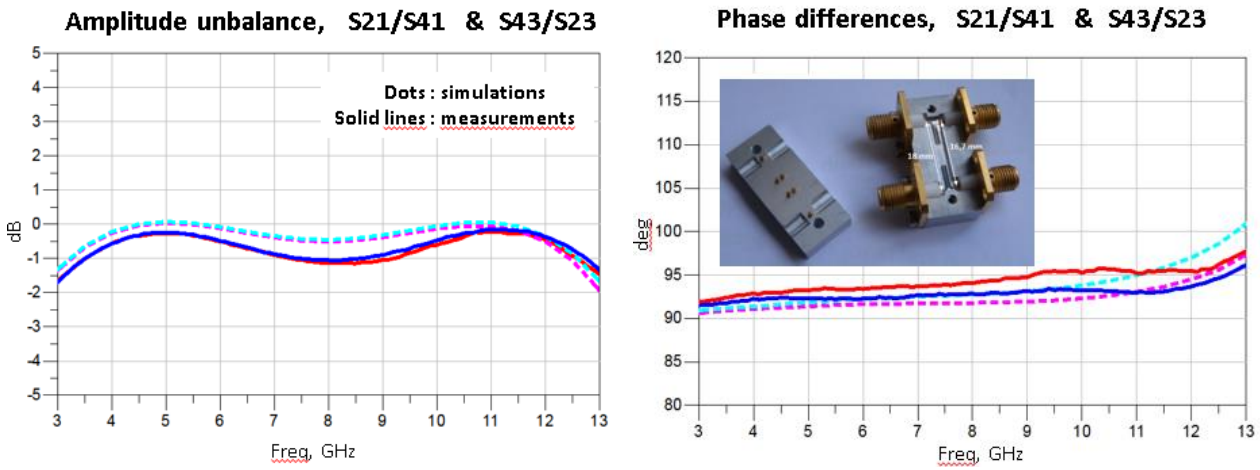

Fig.21: *4-12GHz 3dB 90^0 IF-hybrid coupler. Left: Coupling imbalances. Right: phase imbalances.*

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The baseband LO that has to be supplied at the LO-input of the MMIC is at 1/6 of the fundamental LO frequency in Ku-Band (14.5 – 17.33 GHz) and thus well outside of the IF-band. Figure 22 shows the measurement setup used to characterize the single downconverter test-module, the two synthesizers necessary to generate LO- and RF-signals are not visible on the photo.

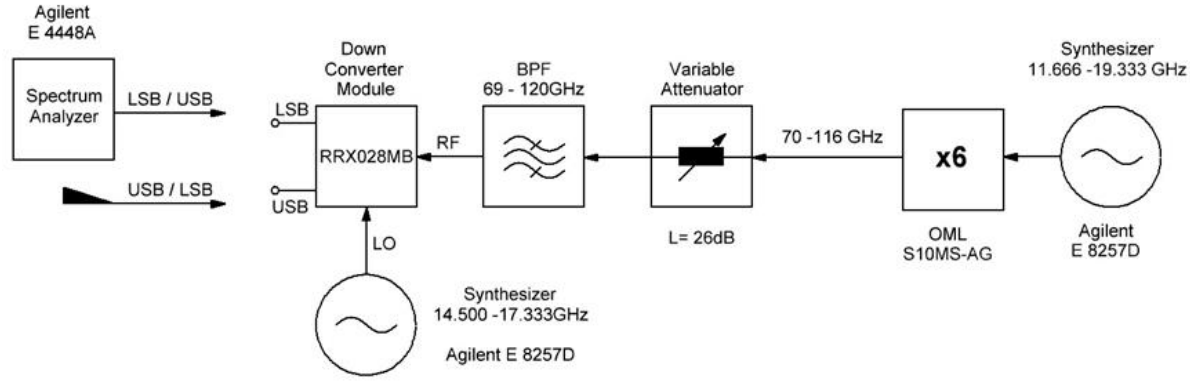

Fig. 22: *Schematic and photograph of the test setup for the downconverter test-module.*

First test was RF-coverage of the module, thus the nominal LSB and USB sidebands were measured for five LO-frequencies and corresponding CW RF-input signals. The resulting coverage of the extended W-band is shown in Figure 23.

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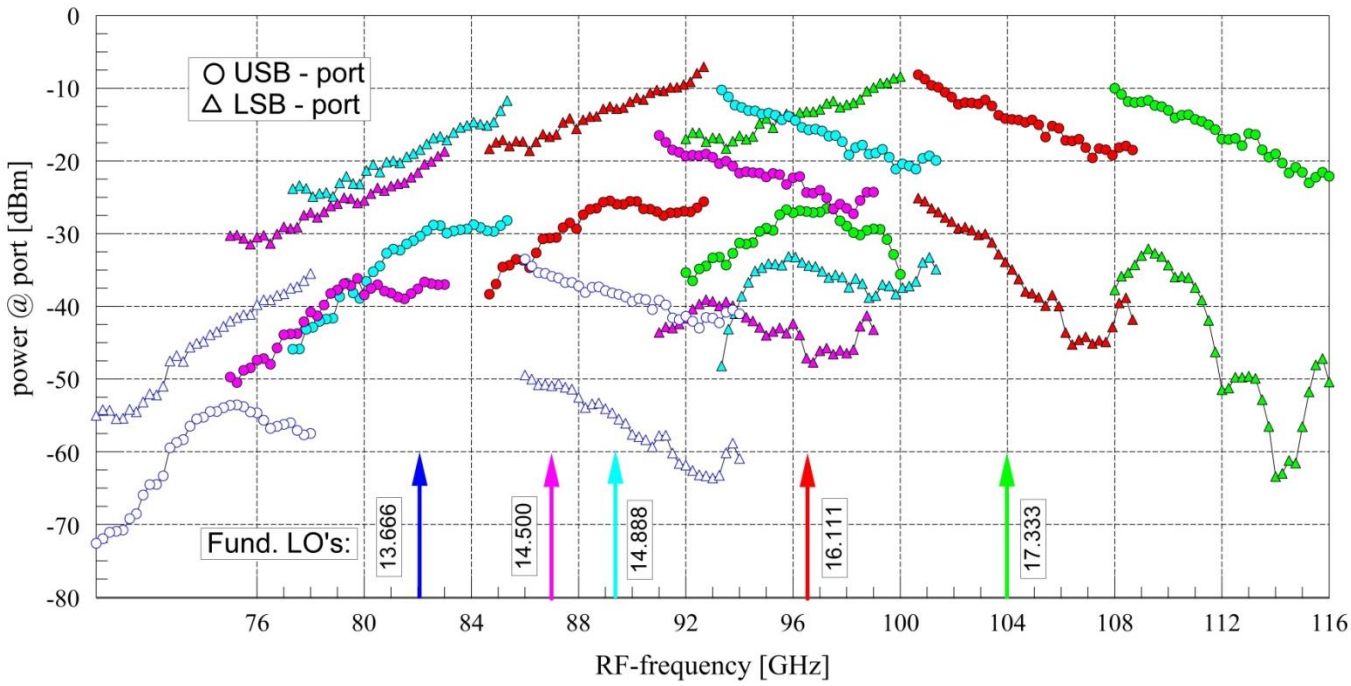

Fig. 23: *Power output at LSB and USB ports of the single downconverter test module for five settings of fundamental LO that cover the full RF-band.*

As can be seen, full coverage of 75-116 GHz is readily achieved using LSB and USB IF-ports. By setting the fundamental LO to 13.666GHz, an attempt was made to extend the covered RF-band down to 67GHz, but doing so IF-power in both sidebands drops by more than 20dB thus preventing use of this fundamental LO-setting. However, a later evaluation showed, that this effect is almost certainly only caused by the on-chip multiplied LO-frequency entering the falling edge of the on-chip LO bandpass-filter – thus the RF-coverage of the chip could probably be extended with a revision of the on-chip LO-filter only.

Next dedicated software controlled measurements were carried out to evaluate the unwanted sideband suppression and suppression of spurs of the multiplied fundamental LO at different LO-setting covering the RF-band 75-116GHz.
Figure 24 shows the measured suppression of the unwanted sidebands measured at LSB and USB ports for four settings of the LO. Unused poerts were terminated into 50Ohm. Suppression measured is mostly 15..20dB with some spots approaching 10dB. It has to be mentioned, that a more exhaustive, computer controlled optimization of the DC-bias of the IF-LNAs could be used to even improve average rejection of the unwanted sideband across the RF-band.

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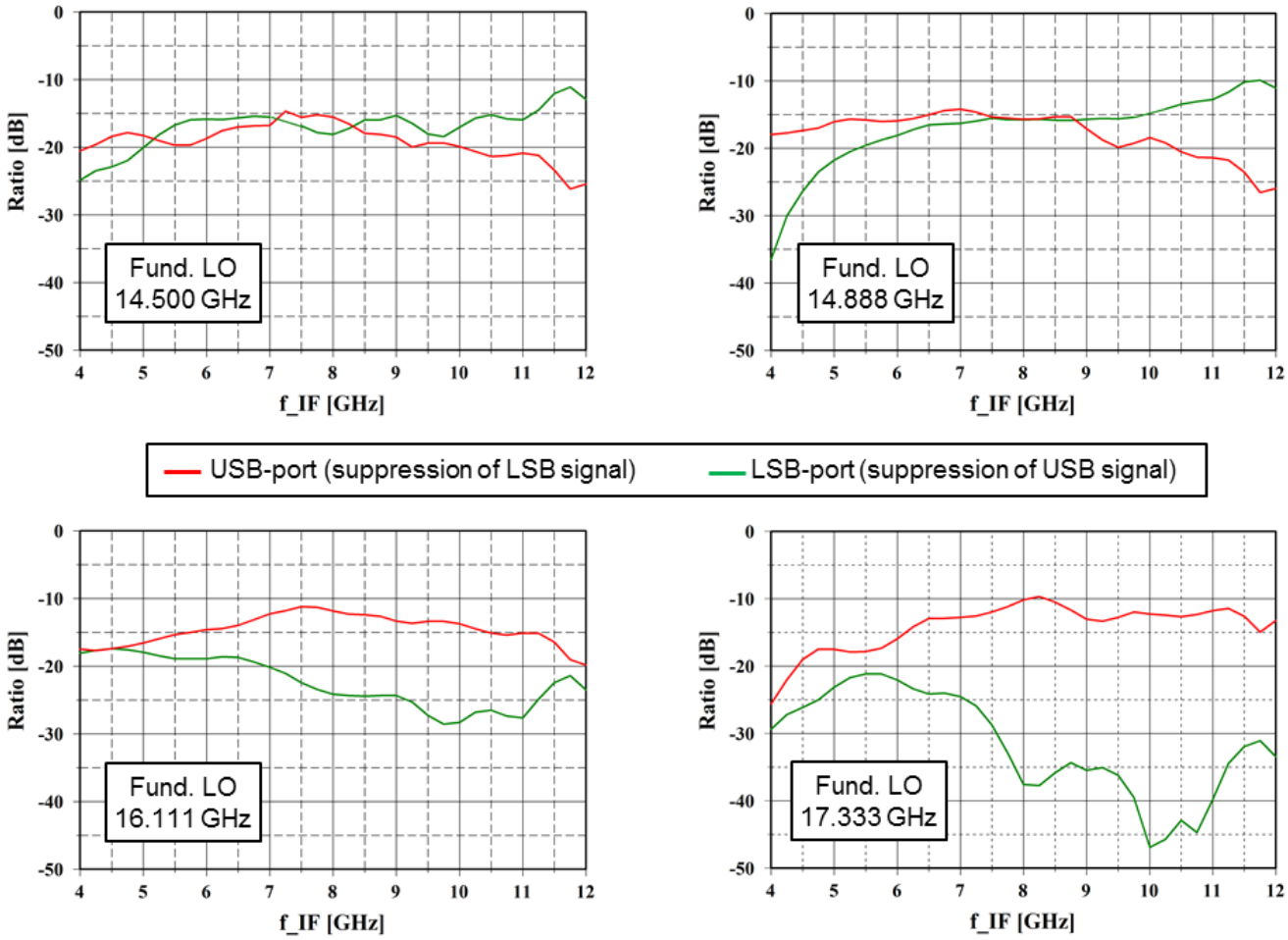

Fig. 24: *Suppression of the unwanted sideband measured at LSB and USB ports for different settings of the fundamental LO.*

Next was evaluation of unwanted harmonic responses of the downconverter chip. Unwanted spurious response is a big problem for wideband tunable downconversion schemes using multiplied LO's. Narrowband filtering of a fixed LO to suppress LO-harmonics, as used with block downconversion schemes employing (several) fixed LO's is not feasible here. Thus several measures to possibly minimize spurious responses have been implemented already with the design of the downconverter chip (antiparallel diode tripler, subharmonic mixer, careful LO-filter design) as described in section 3.1. As can be seen from Figure 25, showing the measured spurious responses, this approach was very successful, spurious response over the full RF-band mostly stays well below ~-30dB, only few spots approaching -20dB. In the graphs squares indicate (wanted) response from the nominal X6 fundamental LO with the proper sideband for the respective USB or LSB port providing the highest level. Next response is the unwanted sideband of the respective USB or LSB port, other harmonic responses (fund. LO x4, x5, x6, x7, each with both sidebands) usually are far off. As with sideband suppression, average unwanted harmonic response across the RF-band could also be further optimized by computer-controlled optimization of IF-LNA DC-bias.

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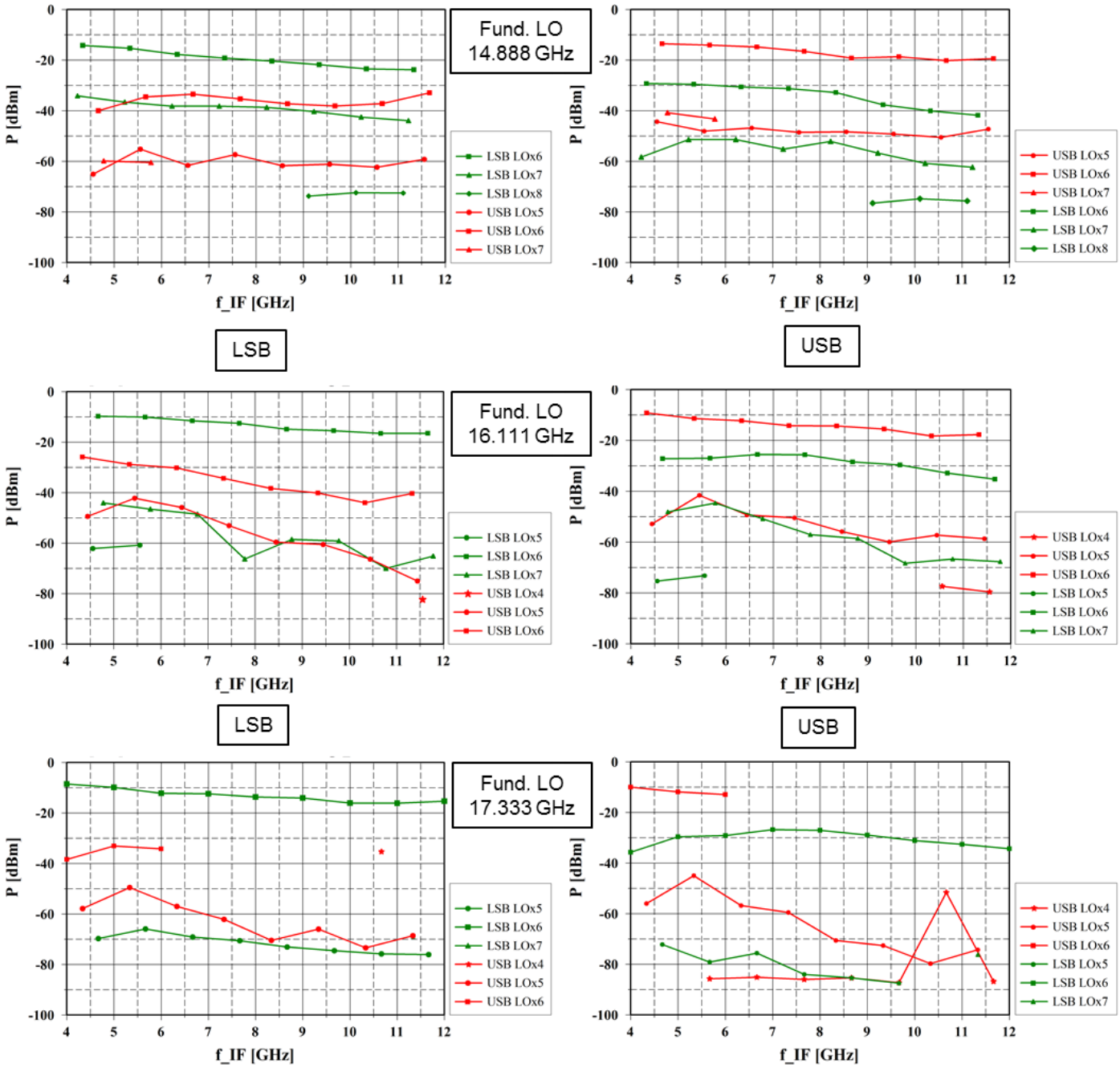

Fig. 25: *Spurious responses of the downconverter chip at LO-harmonics other than fundamental LOx6. Gaps in the data are due to the measurement procedure, the RF-band was covered in 1GHz steps only. In addition an RF-band of only 75-110(!) GHz was covered within this measurement.*

4 Downconverter block for 3 pixels / 6 channels

After successful testing of a single downconverter MMIC, the design of the highly integrated 3 pixel downconverter module was finalized and fabricated. It is made-up from 3 parts and contains hybrids for baseband-LO distribution to the MMIC's, 6 fully integrated downconverter MMIC's, 6 hybrids for 12 LSB/USB IF-outputs, waveguide RF-distribution and DC-bias circuitry. The six RF-inputs to the module shown in Figure 26 are realized using a single custom flange carrying six WR10 waveguides.

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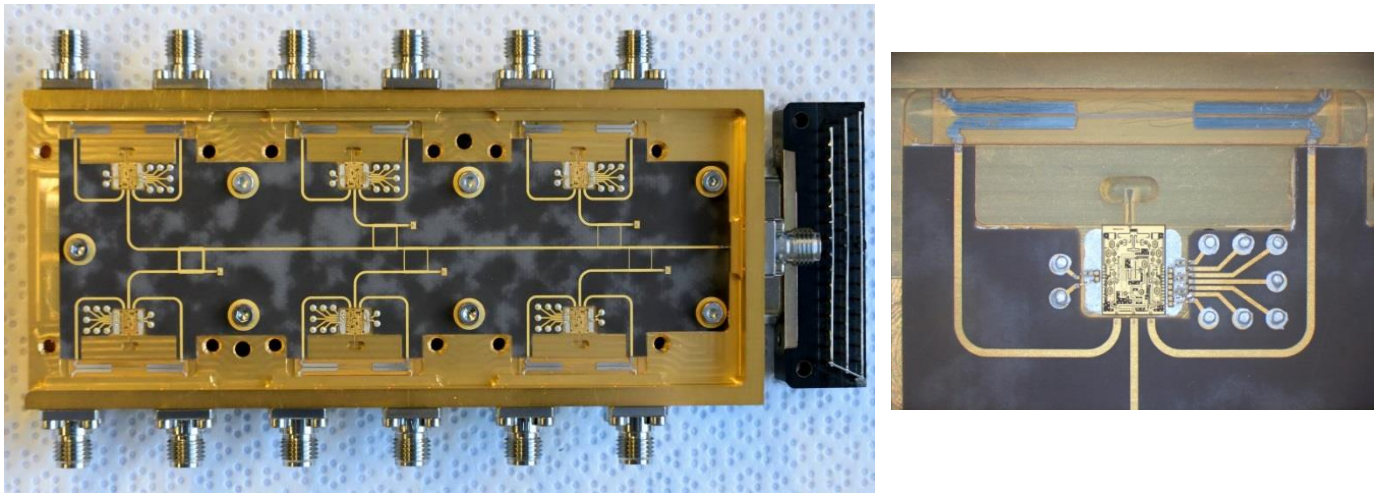

Fig. 26: *Left: Three-pixel downconverter incorporating six fully integrated downconverter MMICs.*
Right: Close-up to one channel showing IF-hybrid on quartz, RF input-waveguide with E-field probe, downconverter MMIC and PCB for routing of LO- / IF-signals and DC-bias for MMIC.

In order to define the RF-band six 68-119 GHz waveguide filters are integrated into a single split-block and connected to the input of the three-pixel downconverter module using the custom flange. A photograph of this six-fold bandpass filter is shown in Figure 27.

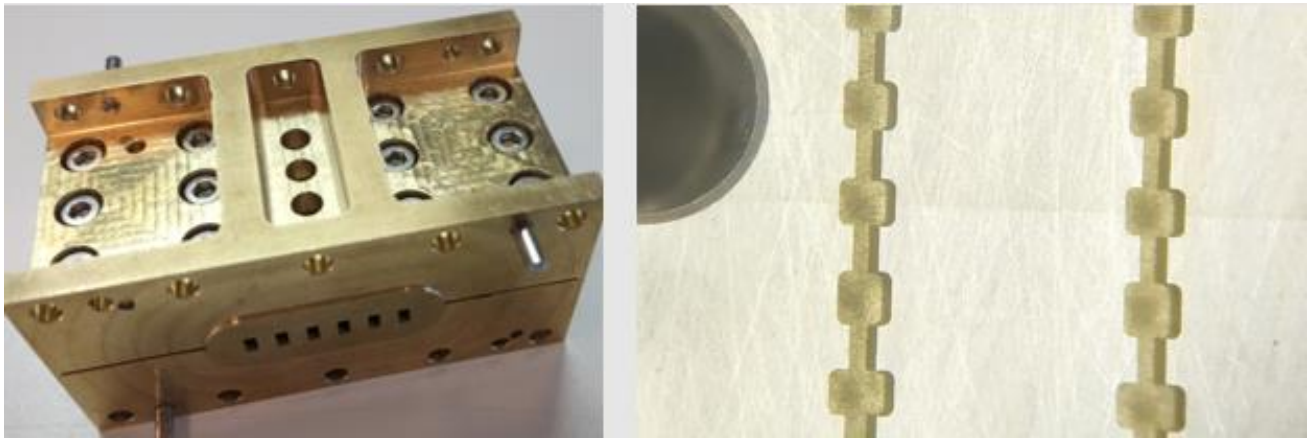

Fig. 27. *Left: Photograph of the 6x waveguide-filter mechanical block with custom flange.*
Right: Zoom-in on the filter cavities.

For distribution of the fundamental LO (14.5 – 17.333 GHz) to the six downconverter MMICs a cascade of branchline couplers was employed. The LO distribution circuitry was designed and tested using a test PCB which is shown in Figure 28 together with measurement of S-parameters. As can be seen, an evenly distribution of LO-power within +/- 1dB is obtained.

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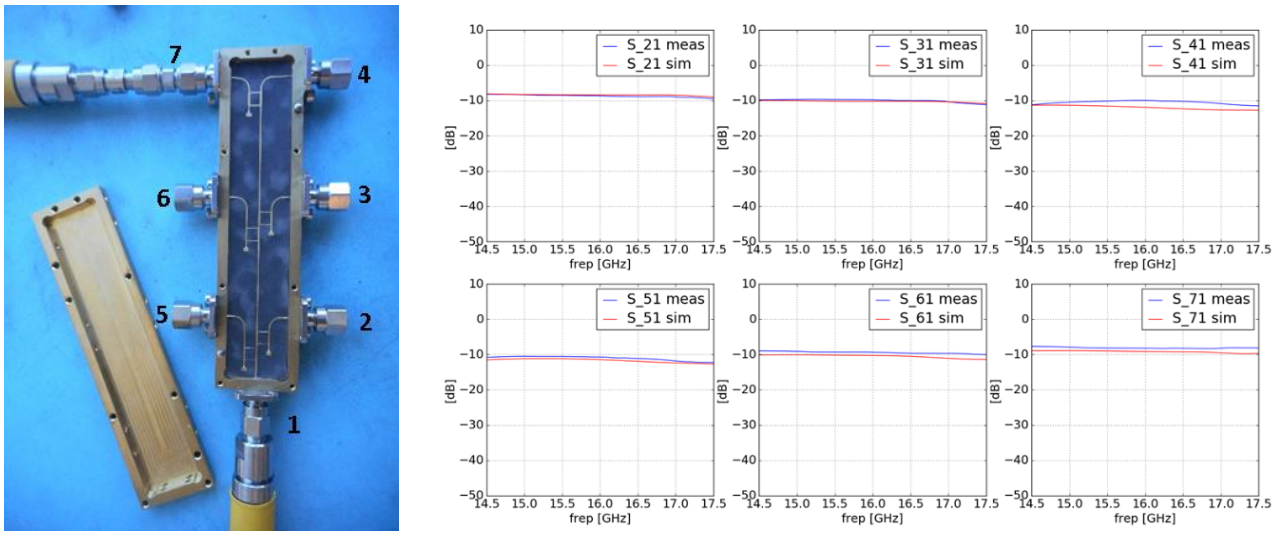

Fig. 28. *Left: Picture of the LO distribution coupler. Right: S-parameters of device.*

5 Array demonstrator

The cryostat was designed to hold an array of 9 pixels arranged in three lines with three pixels per line. An off-the shelf CTI350 cryocooler serves to deliver an end temperature < 15K for the array of pixel modules and ~70K for the radiation-shield. Optics of the system is designed for operation on IRAM's 30m telescope on Pico Veleta, Spain.

5.1 Cryostat -optics, -mechanical & -electrical design

The optical design of the 3x3 receiver array is based on purely reflective optics cooled to cryogenic temperature. It is composed of nine dual-polarizations (linear) corrugated feed horns with circular waveguide inputs. A short square-to-circular transition serves to match the feed waveguide with the (square) OMT waveguide.

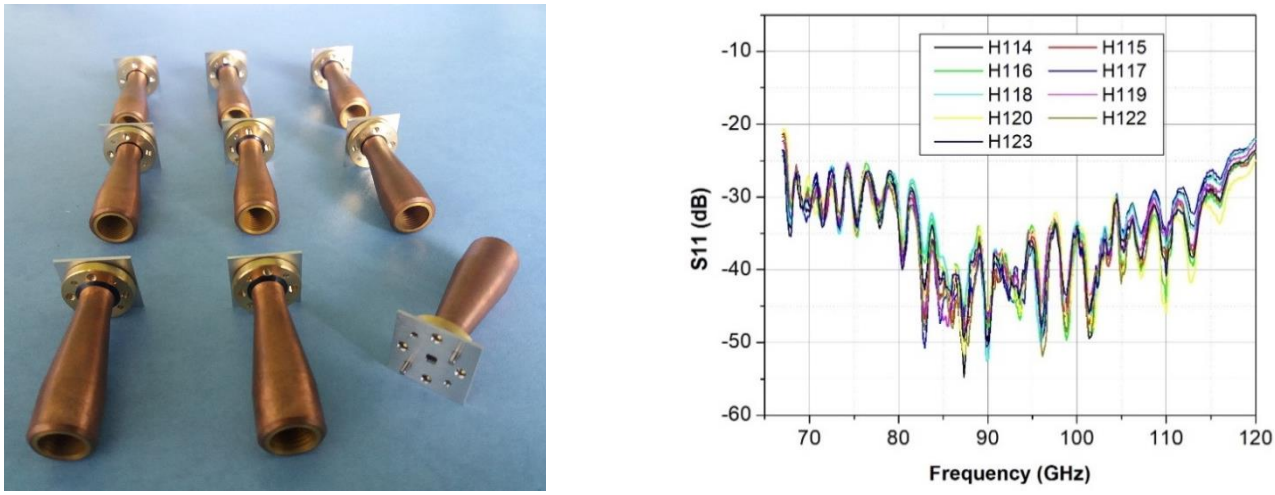

Fig. 29. *Left: Corrugated feed horns for array. Right: Associated return loss measurement.*

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In front of each line of three feeds, a corresponding line of three double-face mirrors is mounted, folding the beams two times 90°. For each horn first mirror face is a flat mirror the second face is a curved mirrors that re-images the sub-reflector onto each horn aperture. In this array of double face mirrors, the flat side of a line of mirrors is used for a certain row of three pixels, whereas the curved side of the line serves the adjacent row of three pixels. Figure 30 shows a photograph of the array of mirrors mounted onto the 15K stage of the cryostat.

Fig. 30: *View of the array of double face mirrors, located inside the cryostat*

A vacuum window with anti-reflection grooves, made from HDPE, and an infrared filter with anti-reflection grooves, mounted to the 70K stage and made from PTFE, were designed and tested. Figure 31 shows a photograph of the fabricated components, whereas in Figure 32 the result from the simulation of the optimized reflection coefficient for the cascade of both components is depicted.

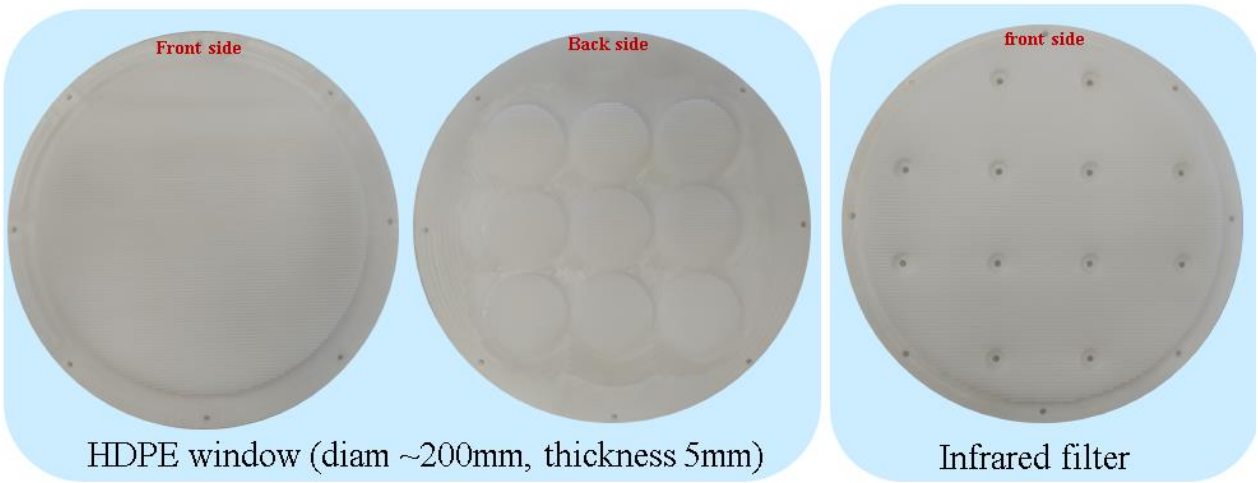

Fig. 31. *<u>Left:</u> Front and back side of machined HDPE window. <u>Right:</u> Machined PTFE infrared filter.*

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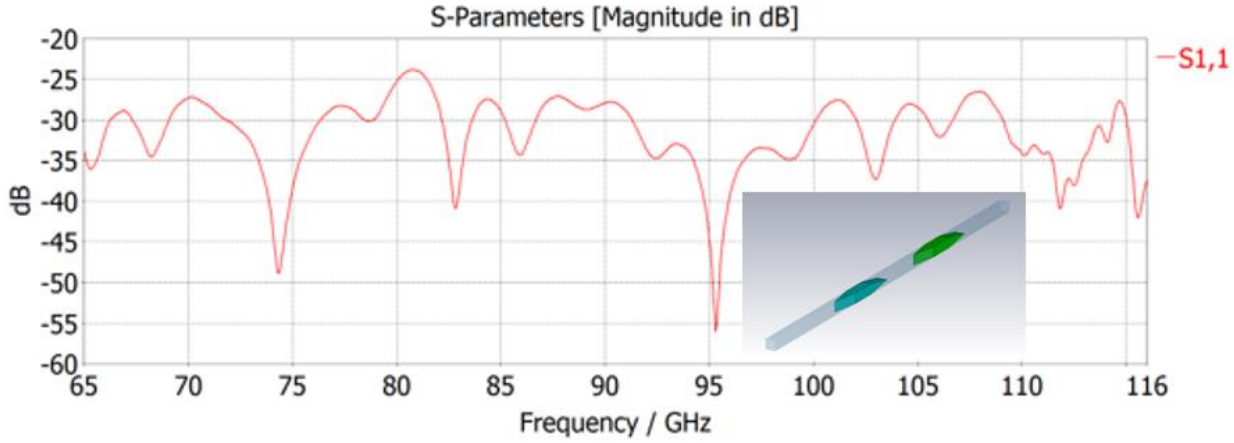

Fig. 32: *Reflection coefficient of the PTFE infrared filter cascaded with the HDPE vacuum window.*

In front of the cryostat window, a Gaussian-beam telescope at ambient temperature serves to provide an edge illumination of -11dB on the subreflector of the 30m telescope. The two focusing mirrors have bi-conical surfaces and were optimized using a raytracing software (ZEMAX). Subsequently the resulting optical system, shown in Figure 33, was analyzed using a field-solver (CST Microwave Studio).

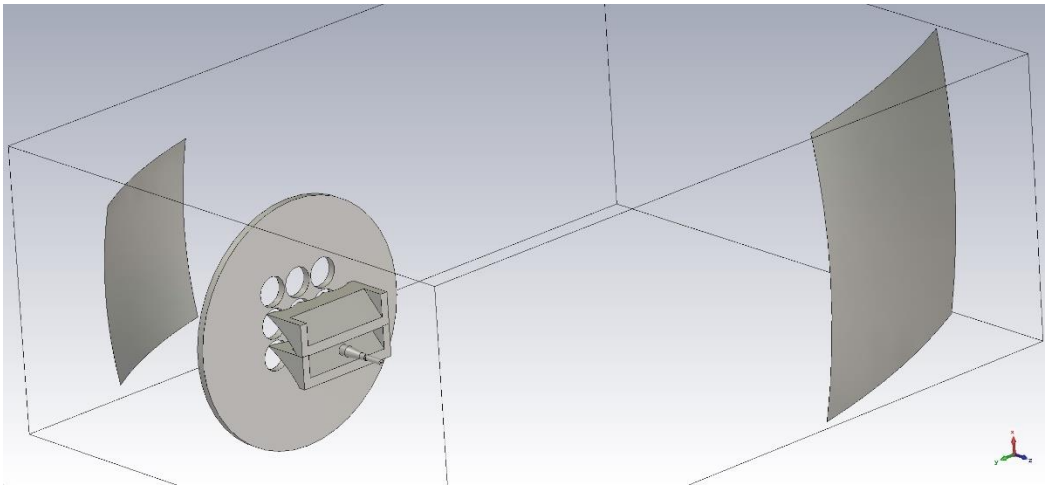

Fig. 33: *Full optics structure, simulated with CST/ Microwave Studio.*

The two far-field cuts of the resulting beam of the cetral pixel of the array, shown in Figure 34 over the RF-band of the system, indicate a frequency-independent illumination of the subreflector.

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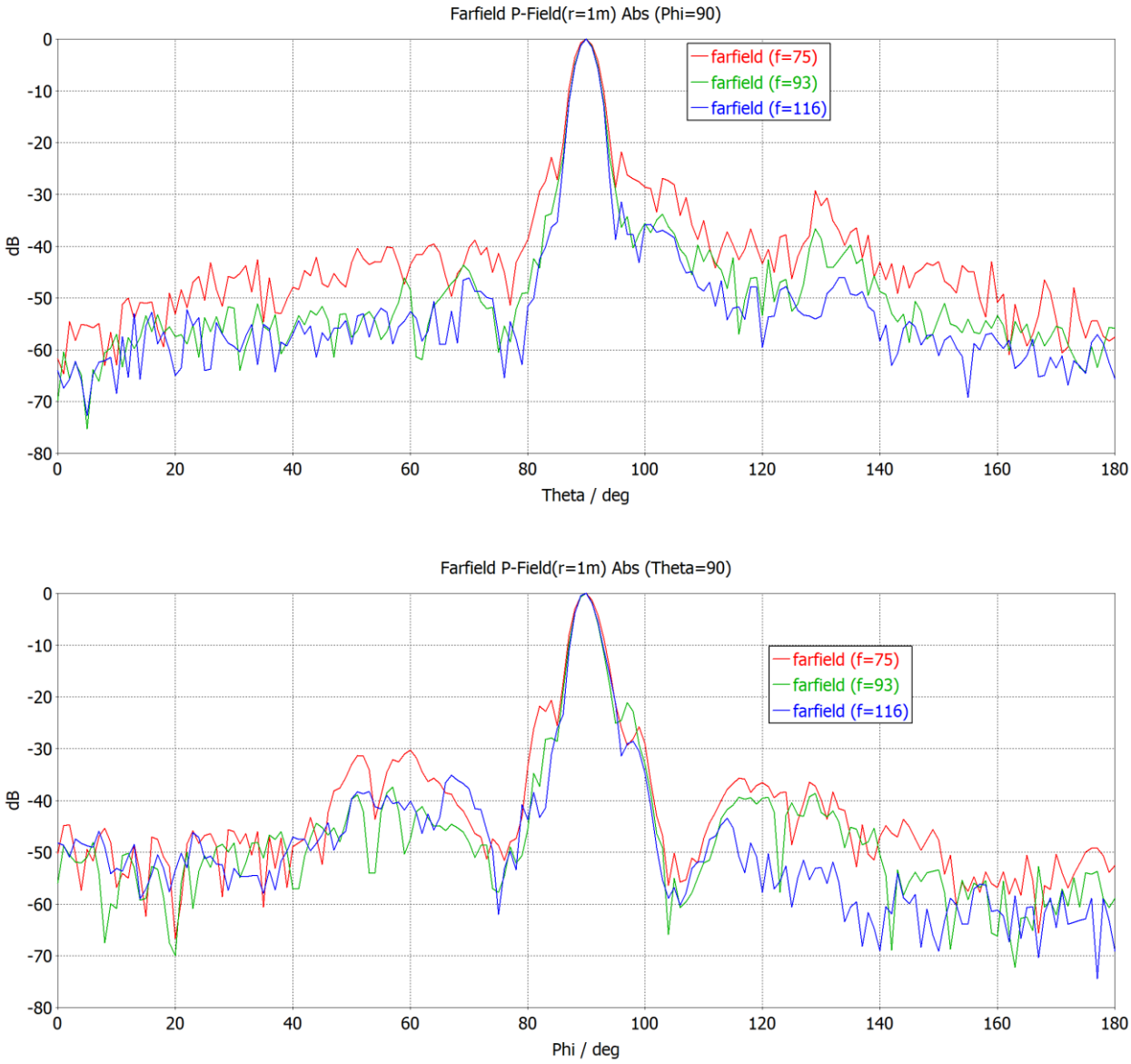

Fig. 34: *Far fields cuts @ 75GHz, 93GHz and 116GHz simulated for the central pixel.*

For the demonstrator array a cryostat based on a Helium closed-cycle CTI 350 refrigerator was designed and manufactured. It provides two temperatures: 77K serving a radiation shield, an infrared filter and heat sinking for DC and RF connections and a 15 K stage to which the 3x3 array and the reflective optics inside the cryostat are attached. To provide a good serviceability of the system, the single-pixel modules are attached to a common copper baseplate that delivers cooling power to the modules and provides the WR10 waveguide connections to the outputs of the pixel-modules. This allows for an easy replacement of single-pixel modules.

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In Figure 35, a cut-away 3D-drawing of the cryostat depicting these features is shown.

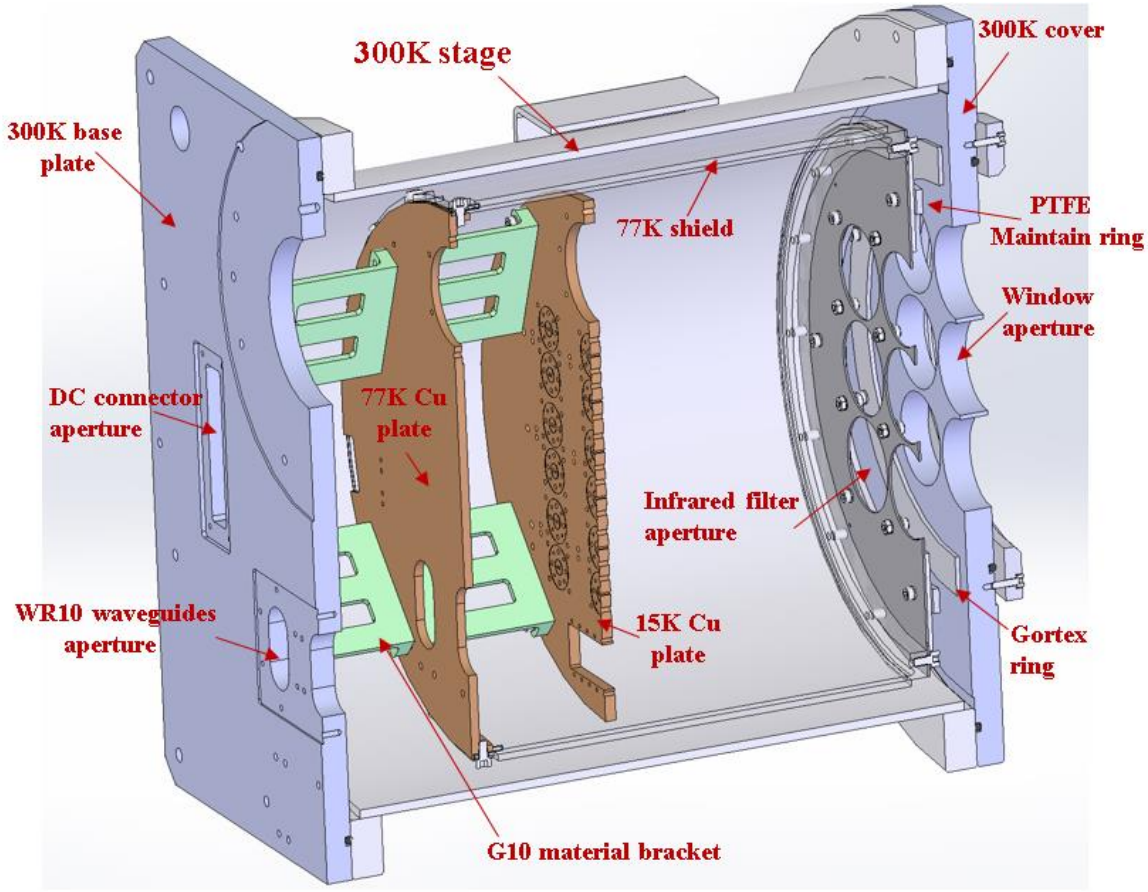

Fig 35: *3D-drawing illustrating the manufactured cryostat.*

Transport of the RF signals from the 15K copper baseplate carrying the single pixel modules to the dewar faceplate is done using three assemblies of six WR-10 stainless-steel waveguides with standard UG387 flanges connecting to the copper baseplate. Lengths of the waveguides is about 150 mm on average, so a good thermal isolation can be achieved and the measured losses (at 300K) are still tolerable, amounting to -7dB to -3 dB as function of waveguide length and frequency. At the ambient temperature output side the six waveguides are combined on the aforementioned custom flange, Figure 36 shows the resulting waveguide harness for a line of three pixels. As an additional benefit, grouping the waveguides into these assemblies largely faciliates assembly of the cryostat hardware.

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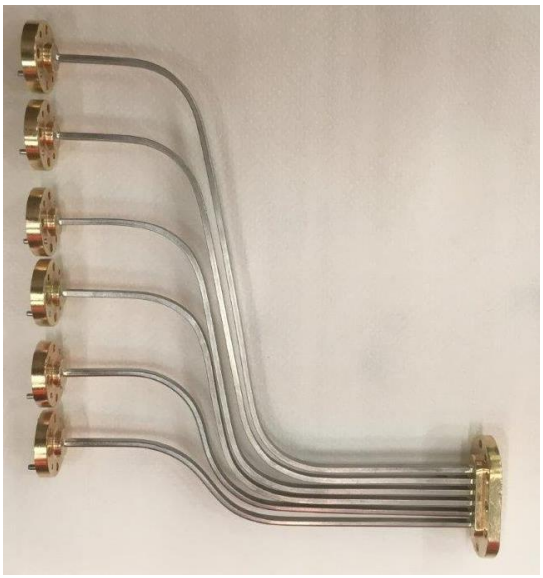

Fig. 36: *WR-10 stainless-steel waveguide harness serving a line of three single-pixel modules.*

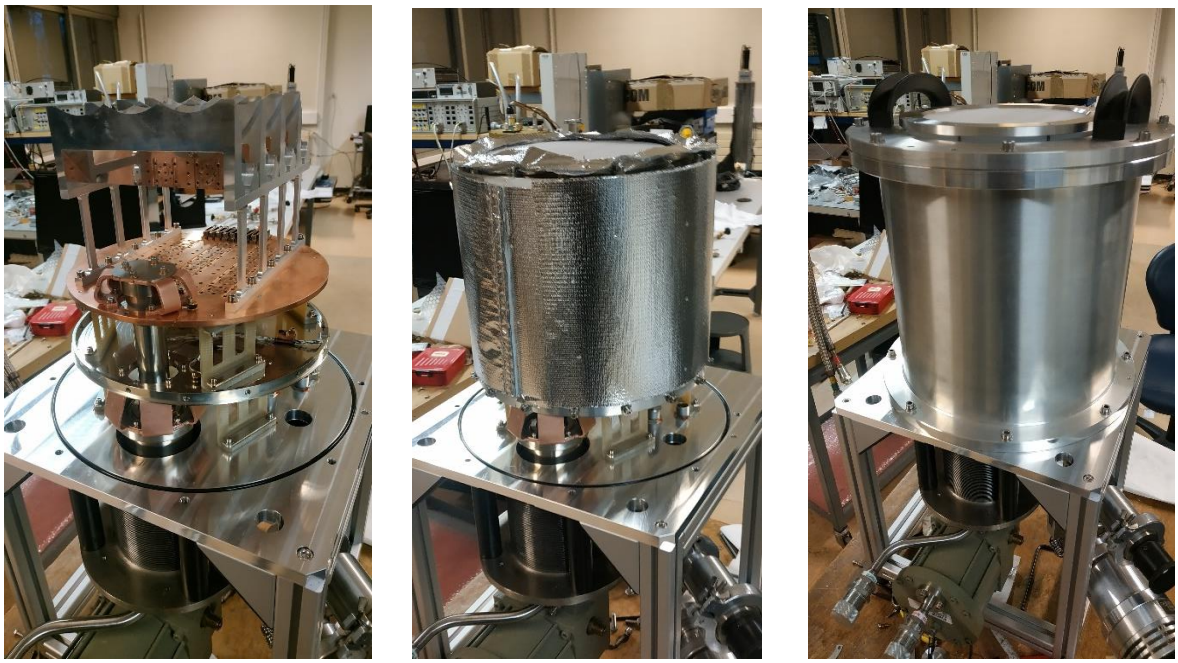

Fig. 37. *Left: 15K stage with copper mounting plate for array, reflective optics attached and 77K stage. Middle: 77K radiation shield with PTFE infrared filter window. Right: Dewar closed, vacuum window on top.*

Figure 37 gives an overview of the assembly of the final cryostat that was manufactured by an external company.The vacuum & cooling performance of the system is excellent: A vaccum level of about $3x10^{-4}$ mbar was achieved at room temperature with all components mounted using a turbo-pump. About $1x10^{-6}$ mbar was obtained for the sealed system cooled to 15K. A recording of a cool-down cycle of the system is shown in Figure 38. Stable conditions are reached after ~12h with all components mounted, wires and waveguides attached. Thereafter temperature variations of the 15K stage within a one-hour time sample are about 20mK only. Upon DC-biasing one single pixel module, the temperature of the 15K stage increased about 0.1K, thus a temperature on the 2nd stage of ~13K is expected in the case of nine pixels biased.

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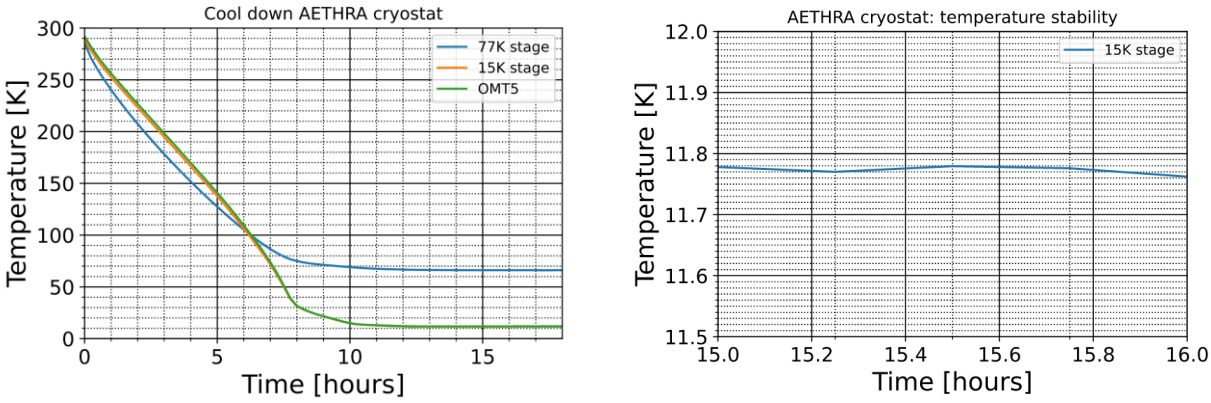

Fig. 38. *Left: WP5.1 cryostat cool down recording. Right: Zoom-in on 1h temperature recording of the 15K stage after thermalization of the system.*

5.2 DC-bias system for array demonstrator

The array demonstrator is monitored and controlled through the M&C rack, a 19” x 3U standard rack that incorporates two different types of electronic bias boards: the GAIA board and the PSG board (see Fig 6), used respectively for the cryogenic MMIC low noise amplifiers of the active OMT module and for the room-temperature downconverter.

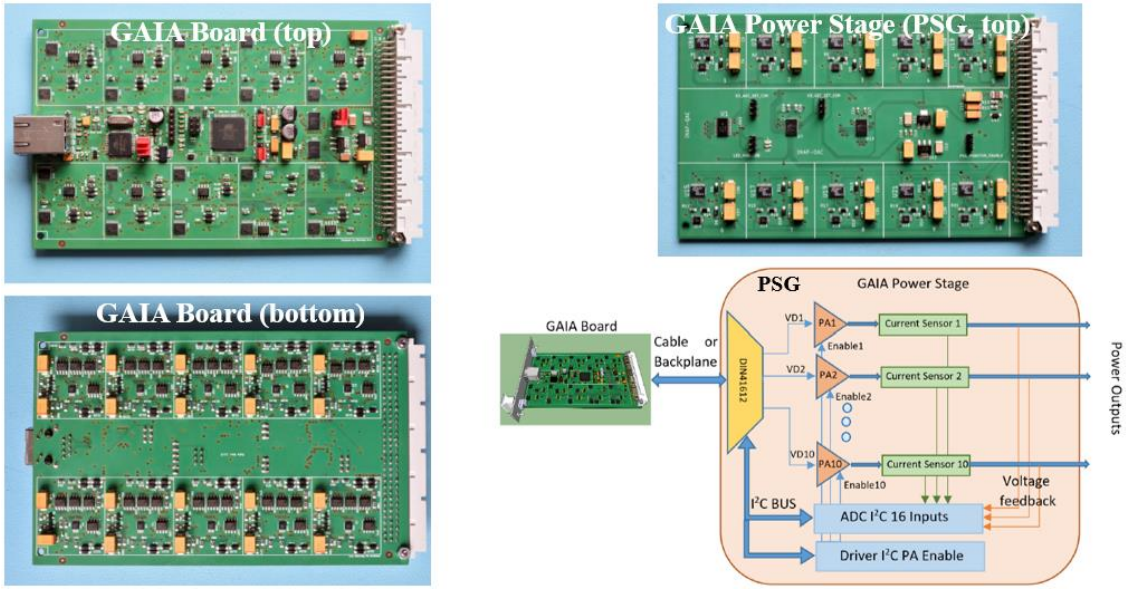

Fig. 35: *Left: GAIA digital bias board of cryogenic MMIC LNAs (top and bottom views). Top right: Power Stage of GAIA board (PSG) of MMIC downconverter. Bottom right: Schematic of GAIA board cascaded with PSG.*

The GAIA board (Fig. 35, left panel) is a four-layer rack-mountable programmable digital bias board based on a microcontroller and on digital potentiometers designed for biasing, remote monitor and

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control of the gate voltages V_g and of the drain voltages V_d of cryogenic Low Noise Amplifier (LNA) modules. One single GAIA board can control up to 10 × V_d and 10 × V_g and monitor 10 × V_d, 10 × V_g and 10 drain currents, 10 × I_d. The Id of each LNA module amplification stage is imposed by the assigned V_d and V_g. The digital board is designed to provide high bias voltage stability and proved to generate very low RFI emission, as required for radio astronomy purposes. The procedure for setting up the bias voltages to their goal values, when switching on the LNAs, is reached incrementally from the zero-volt condition and is coded in the microcontroller firmware. The inverse procedure is applied when switching off. The same board includes analogue to digital converters for remotely monitoring V_d, V_g and Id for each of the 10 channels.

Table 1 shows the main electrical specifications of GAIA, including the bias limits. An RJ45 port is available on the board front panel for communication. The ultra-stable gate and drain voltages are available at the board outputs pins of a DIN 41612 male connector. The GAIA board can deliver a maximum drain current of Id=50 mA, with a drain voltage V_d=5 V. The voltage resolution is ≈4.8 mV for V_d and ≈11.2 mV for V_g.

Item	Values
N. of amplification stages	10 (10 × V_d and 10 × V_g)
Drain voltage range	0 V ≤V_d≤ 5 V
Gate voltage range	-6.5 V ≤V_g≤ 5 V
Maximum drain current	I_{dmax}≤ 50 mA (per channel)
Max total power consumption	≈5 W (≈2.5 W for GAIA board + ≈2.5 W for LNA load)
ADC characteristics	16 bit with ≈15 Hz sampling rate
Voltage resolution setting	≈4.8 mV for V_d, ≈11.2 mV for V_g
Communication port	Auto-negotiated 100 Mb LAN with RJ45 connector
Board size (without front panel)	h=100 mm, depth=160 mm

Table 1: *Main specification of the GAIA digital LNA bias board.*

Item	Values
N. of amplification stages	10 × V_d
Drain voltage range	0 V ≤V_d≤ 5 V
Maximum drain current	I_{dmax}≤ 500 mA (per channel)
Max total power consumption	≈50 W (≈25 W for PSG board + ≈25 W for downconverter load)
ADC characteristics	16 bit with ≈15 Hz sampling rate
Voltage resolution setting	≈5 mV
Communication port	Serial port I^2C for communication with GAIA board
Board size (without front panel)	h=100 mm, depth=160 mm

Table 2: *Main specifications of the PSG (power stage of GAIA board).*

The GAIA board cannot be employed to monitor and control the AETHRA WP1 75-116 GHz downconverter module as the power amplifiers of the fully-integrated MMICs require current values of

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up to 300 mA each (≈6 times greater than what GAIA can deliver). Therefore, a power stage of the GAIA board was developed to comply with the high-current bias requirements of the AETHRA WP1 downconverter. The power stage of the GAIA board (Figure 35, right panel), named PSG (Power Stage Gaia), is a four-layer digital bias board connected in series with GAIA, capable of delivering up to 10 × high-current stages with I_{dmax}=500 mA per channel. The main specifications of the PSG are summarized in Table 2. One GAIA board is used to monitor and control one PSG board. The latter is an extension of GAIA and cannot be used independently from it. Therefore, one GAIA board plus one PSG board must be used in conjunction to monitor and control up to 10 high-current stages of the AETHRA WP1 downconverter. A block diagram of the PSG, showing its interconnection to the GAIA board, is shown in Figure 35, bottom right panel. The PSG main components are 10 power amplifiers (PAs), 10 current sensors, two Analog-to-Digital Converters (ADCs) and one driver, managed by I2C bus. The components are mounted on a 100 mm ×160 mm Eurocard board with size identical to GAIA.The bias schemes of the AETHRA WP1 cryogenic LNA MMICs and downconverter MMIC are shown in Figures 36 and 37, respectively.

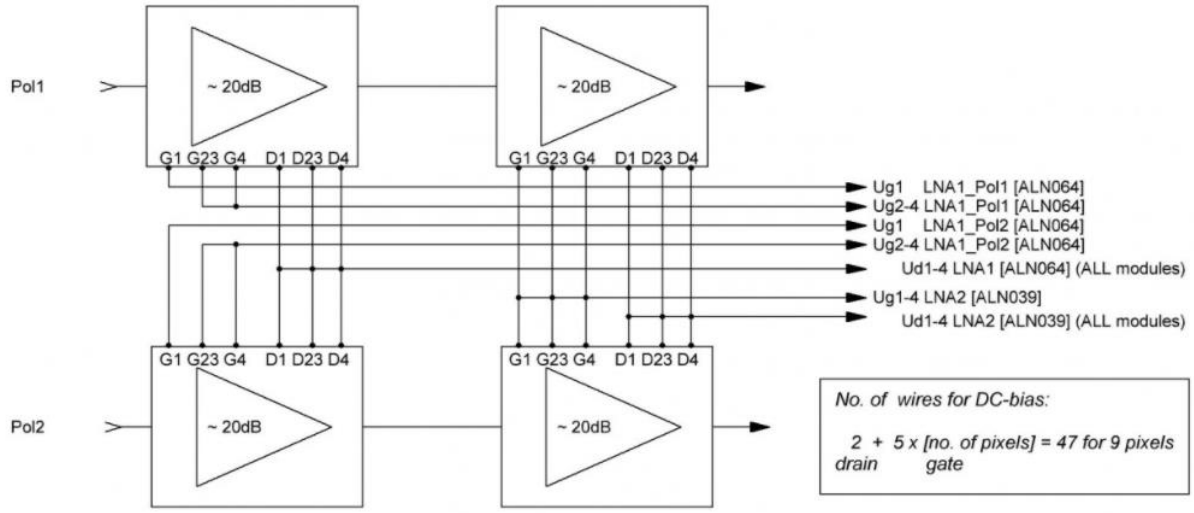

Fig. 36: *Schematic of DC-bias of LNA MMICs of one of the dual polarization pixels of the array.*

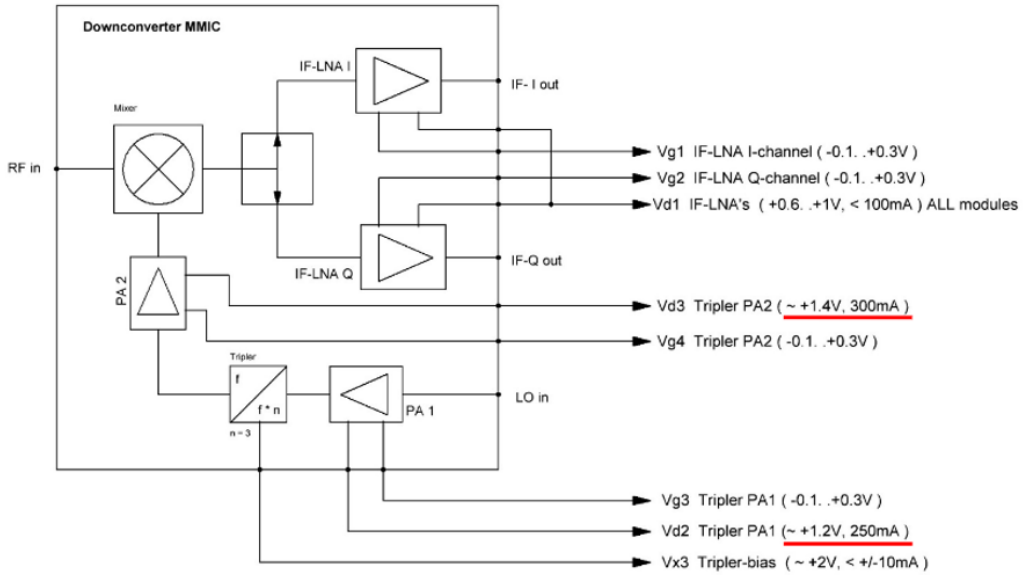

Fig. 37: *Schematic of DC-bias for one downconverter MMIC.*

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The receiver array demonstrator utilizes one single line of three dual-polarization pixels, rather than three lines, as required for the full 3×3 array. The demonstrator has allowed us to validate one of the three-pixel downconverter module. Biasing of the array demonstrator required to bias 39 gates, 3 drains, and 12 power drains, thus requiring to develop a M&C rack with four GAIA boards (GAIA1 - 4) and two PSG boards (PSG1 & 2). Photos of the rack that we developed are shown in Figure 38. The rack incorporates four GAIA boards, two PSG boards and five commercial power supplies for the bias of the electronic boards. Two 1U×19" rack-mountable commercial cooling fans with front switch are also employed, one above and one below the main 3U rack with GAIA and PSG boards. Four DB37 connectors on the rack backplate are used to connect the board signals to the receiver array through a multihead cable (with 71 used wires plus spares). On the receiver side, one MicroD HD51 connector and one SubD HD62 connector are used for the downconverter and active OMT, respectively.

Fig. 38: *Monitor and Control rack of the AETHRA WP1 receiver array demonstrator. The main rack (3U×19") incorporates four GAIA boards, two PSG boards, and five commercial power supplies. Two 1U cooling fans, one above and one below the main rack, are used to maintain a constant airflow through the electronics and avoid over heating of the PSG boards.*

The remote control software of the GAIA and PSG boards allows to operate the boards through a Graphical User Interface (GUI) developed in Python 3.7. The software requires installation of NI VISA Library and runs on Windows 10 OS and Linux. In Windows10, the software is deployed as executable and it does not need installation.

The user can control the four GAIA boards of the array demonstrator, two of which are associated with the PSG boards, from a single GUI. Each tab is uniquely associated to one GAIA board (or GAIA+PSG board) through its IP address. Fig. 39 shows the main window when "GAIA 1" is selected (the example shows that up to 16 GAIA boards can be controlled from the GUI). The board name of each of the GAIA tabs as well as the three identification names under "Channel 01" (in the example "Vd1", "Id1", and "Vg1") can be easily changed by the user through the file "channel_names.cfg", which is automatically uploaded at program start.

The GAIA board firmware and software allows the user to set, for each of the channels, the speed at which a target voltage is reached starting from a default voltage value. Also, the user can decide to disable or to enable how the voltage target value (both for V_d and V_d) is reached: if the button "Enable/Disable V_d without slope" is "disabled" (see below), the V_d target value is reached right after clicking the desired voltage target, while if the button is "enabled" the target value is reached incrementally. Also, the GAIA firmware and software allows to establish the order at which the gate and the drain of each of the channels are biased: if "Enable channel order" is set to "D>G", at the program start, the Drain voltage will be set before the Gate voltage. Vice versa, if "G>D" is set, the Gate voltage

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will be set before the Drain voltage. The GAIA and PSG boards were calibrated in the laboratory before they could be used with the AETHRA receiver array demonstrator.

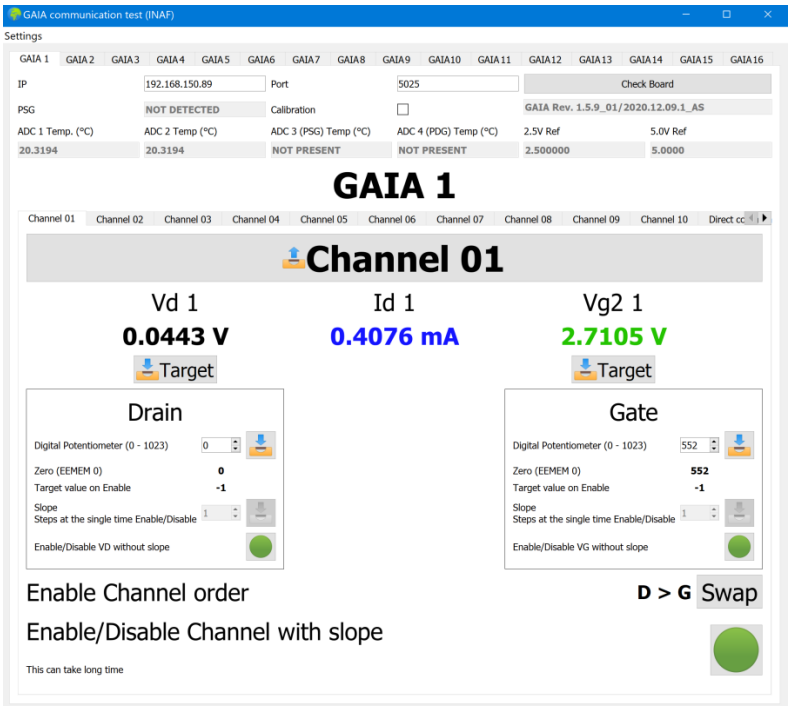

Fig. 39: *Main window of the GAIA and PSG bias boards control software. The GUI allows to monitor and control the Vd and Vg voltages and monitor the Id currents of 10 independent channels of each of the boards. The AETHRA receiver array demonstrator requires M&C of two GAIA boards for the LNAs and two GAIA boards cascaded to two PSG boards for the three-pixel downconverter.*

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5.3 Integration & Tests of full receiver

Last but not least, the WP5.1 Array demonstrator was fully assembled including three single-pixel modules and tests of the full system were carried out at room and cryogenic temperature. Figure 41 finally shows the noise temperature achieved for both polarization channels of the central pixel of the array populated with module SN#2. For this full-band measurement, LSB and USB IF's were recorded upon stepping the LO-frequencies supplied to the three pixel downconverter module to fully cover 75-116GHz.

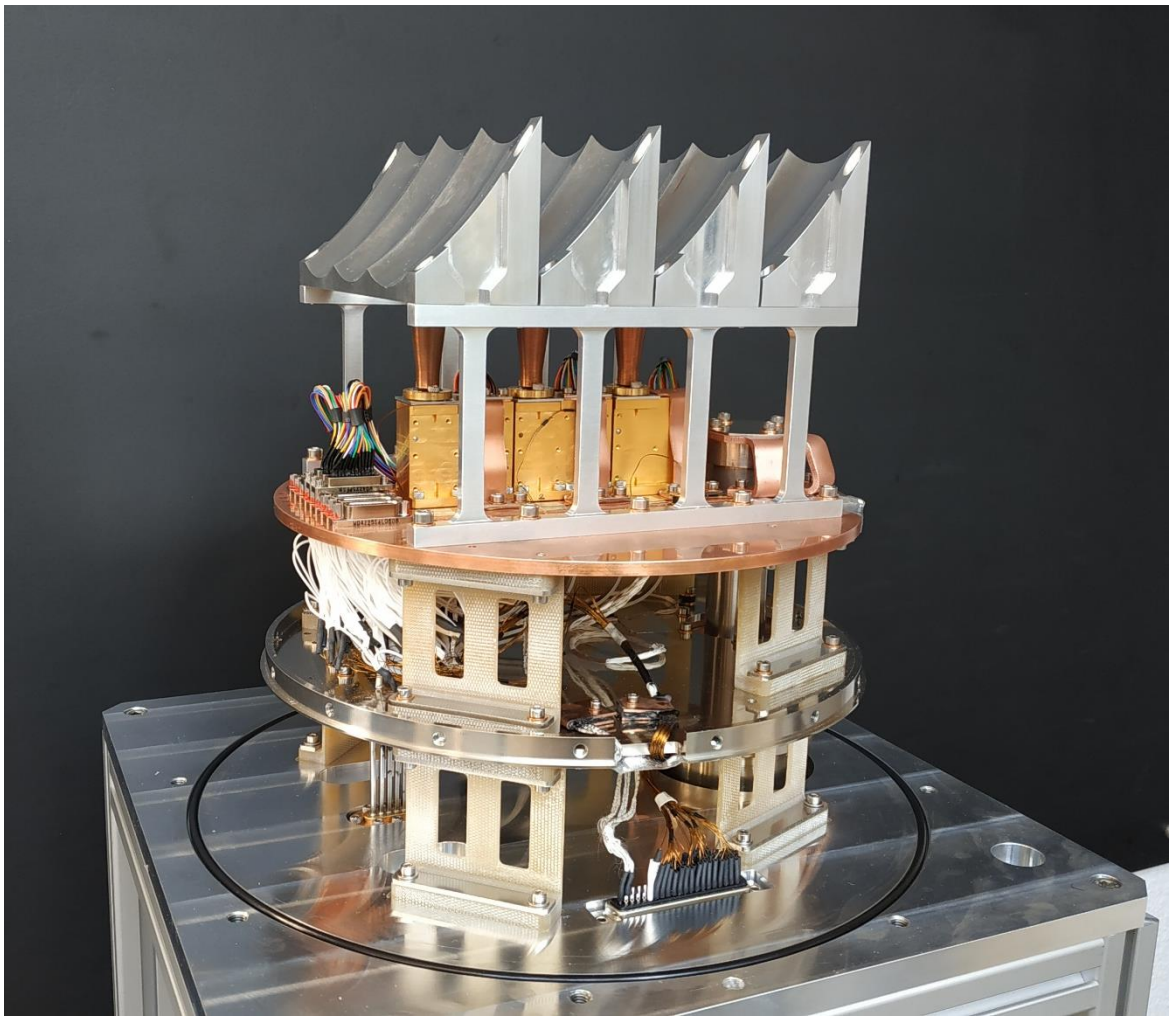

Fig. 40: *WP5.1 Array demonstrator, fully assembled with three single-pixel modules installed.*

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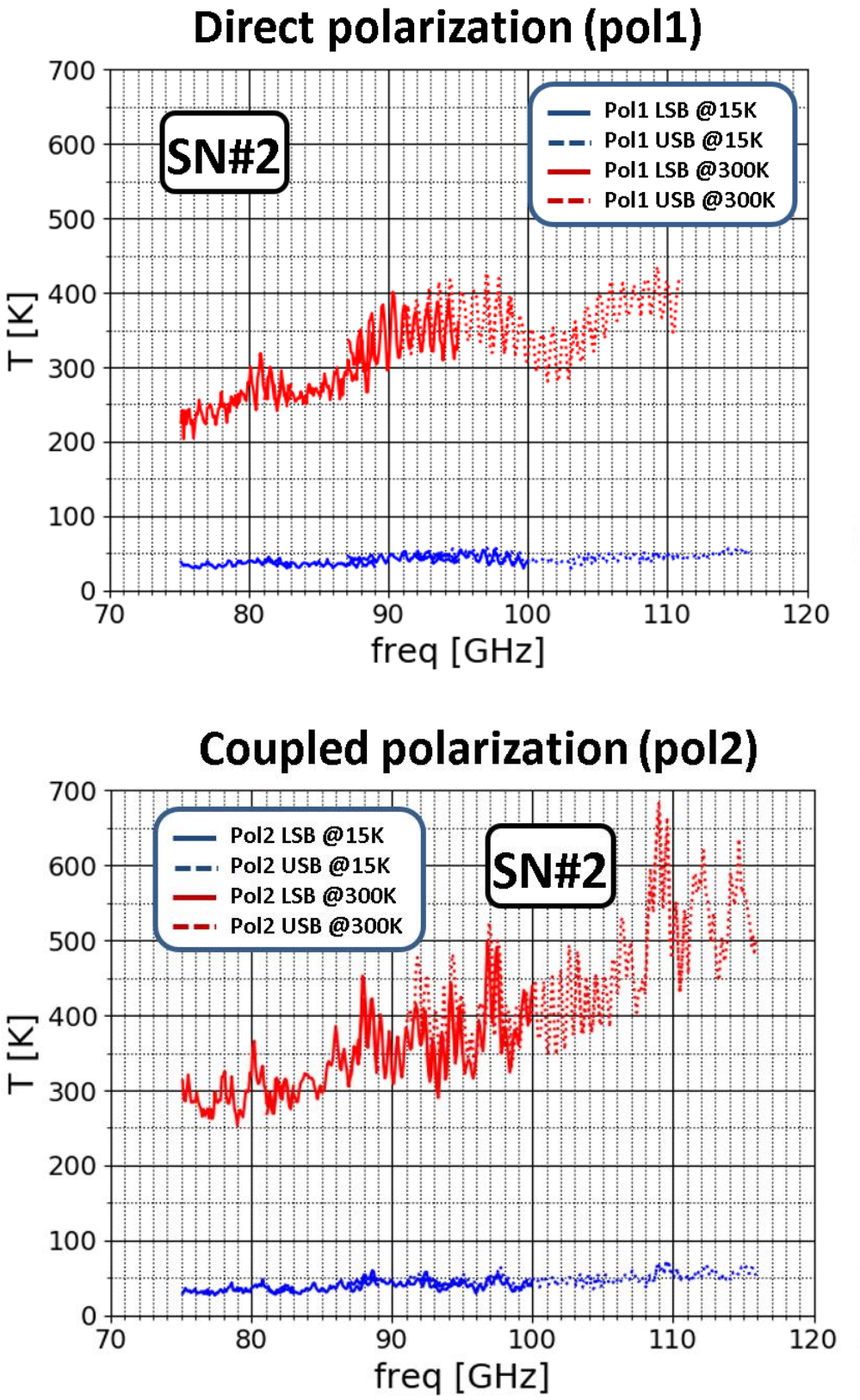

Fig. 41: *WP5.1 Array demonstrator. Noise temperatures for central pixel across full band. LSB and USB IF's displayed, fundamental LO stepped to cover full band.*

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6 Impact of Covid19 pandemic

There was extensive impact of the Covid19 pandemic on WP5.1. The restrictions during almost the entire year 2020 hit the project in the very susceptible phase of component revision and final testing prior to integration of the components. In addition, production of (mechanical) hardware by external companies was also largely delayed if possible at all. Each of the partners suffered from partly or full shutdown of their respective institutions during some periods. Mid 2020 it was decided by RadioNet board, to nevertheless follow the original plan to terminate the JRAs end of 2020 and rather de-scope the agreed descriptions of work and deliverables accordingly. Of course this de-scoping assumed no further shutdown to come before end of the year, and thus was (at least partly) obsolete again by end of October. The detailed impact on our work package, agreed upon with RadioNet, is listed below:

- We had to cancel the planned test of the demo-array at IRAM's 30m telescope and rather do a demonstration in the Lab only.
- Population of the cryostat with pixels was limited to 3 single pixel cryogenic modules and 3 pixel downconverter module.
- Lab demonstration of the module hardware in the demonstrator array was done for 1 pixel and the 2 corresponding downconverter channels only.
- Could not evaluate potential of automatic system optimization with software driving the computer controlled DC-bias for the LNAs and for the downconverter module.

All partners would have been glad to see the demonstrator array on the telescope. Therefore the boundary conditions that might possibly allow to catch-up on this will be evaluated among the partners in the near future.

7 Conclusions

A technology concept for the realization a scalable multi-beam cryogenic receiver array for application in radio-astronomy was developed. Hardware for a demonstrator array, providing 3x3 pixels on-sky when fully assembled, was built and successfully tested in the laboratory - despite the strong restrictions imposed by the Covid19 pandemic. The array architecture is based on two standardized modules that can be stacked to realize arrays of varying geometry and pixel counts. Design of the two modules themselves also follows a highly integrated approach, the core being based on only two highly integrated MMICs. The excellent noise temperature of the employed mature mHEMT technology and the careful optical design of the receiver were proven by the excellent noise temperatures achieved across extended W-band.

8 Publications

[1] F. Thome, A. Leuther, H. Massler, M. Schlechtweg, and O. Ambacher. Comparison of a 35-nm and a 50-nm Gate-Length Metamorphic HEMT Technology for Millimeter-Wave Low-Noise Amplifier MMICs. In *IEEE MTT-S Int. Microw. Symp. Dig.*, pages 752-755, Jun. 2017.

[2] F. Thome, A. Leuther, J. D. Gallego, F. Schäfer, M. Schlechtweg, and O. Ambacher. 70–116-GHz LNAs in 35-nm and 50-nm Gate-Length Metamorphic HEMT Technologies for Cryogenic and Room-Temperature Operation. In *IEEE MTT-S Int. Microw. Symp. Dig.*, pages 1495-1498, Jun. 2018.

[3] G. Valente, A. Navarrini, F. Schaefer, P. Serres, F. Thome, Architecture of Highly Integrated Cryogenic Active Planar OrthoMode Transducer for the 3 mm Band, Proceedings of 2nd URSI AT-RASC, Gran Canaria, 28 May – 1 June 2018.

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[4] A. Navarrini, G. Valente, P. Serres, F. Schaefer, F. Thome, O. Garnier, Compact Dual-Polarization Cryogenic Receiver Module for the 75-116 GHz Band, 2018 IEEE International Conference on Electromagnetics in Advanced Applications (ICEAA), Cartagena de Indias, Colombia, Sep. 10-14, 2018, pp 479-482.

[5] F. Thome, A. Leuther, F. Heinz, and O. Ambacher. W-Band LNA MMICs Based on a Noise-Optimized 50-nm Gate-Length Metamorphic HEMT Technology. In *IEEE MTT-S Int. Microw. Symp. Dig.*, pages 168-171, Jun. 2019.

[6] F. Thome, E. Ture, R. Iannucci, A. Leuther, F. Schäfer, A. Navarrini, and P. Serres. Frequency Multiplier and Mixer MMICs Based on a Metamorphic HEMT Technology Including Schottky Diodes. In IEEE Access, vol. 8, pages 12697-12712, 2020, DOI: 10.1109/ACCESS.2020.2965823.

[7] F. Thome, E. Ture, A. Leuther, F. Schäfer, A. Navarrini, P. Serres, and O. Ambacher. A Fully-Integrated W-Band I/Q-Down-Conversion MMIC for Use in Radio Astronomical Multi-Pixel Receivers. In IEEE MTT-S Int. Microw. Symp. Dig., pages 193-196, Aug. 2020, DOI: 10.1109/IMS30576.2020.9223856.

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