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Low noise, cryogenic 35nm mHEMT MMIC amplifiers

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Authors (Institutes)	Fabian Thome (Fraunhofer IAF)

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1 Introduction

As part of the work package 5.1, the deliverable D5.2 describes the evaluation of the cryogenic performance of the Fraunhofer IAF 35-nm gate-length mHEMT technology and the comparison to the more established 50-nm gate-length mHEMT technology. Based on the application, the target frequency range is from 72 to 116 GHz.

During the last decade, a lot of effort was put into the scaling of the gate length of HEMT technologies in order to increase the operating frequency and to improve the noise performance. Thereby, InGaAs-based HEMTs, such as the so-called InP HEMTs and mHEMTs, achieve the best noise temperatures, both at room and cryogenic temperatures.

The following results are also part of publications [1]-[3] that were published under the framework of RadioNet and are open accessible.

2 Available 35-nm and 50-nm mHEMT Technologies at the Beginning of the Project

The presented MMICs are based on a 35-nm and a 50-nm gate-length mHEMT technology [4], [5]. For a lattice-matched growth of the HEMT layers on 4-inch semi-insulating GaAs wafers, a linear graded $In_xAl_{0.48}Ga_{0.52-x}As$ ($x = 0 \rightarrow 0.52$) metamorphic buffer is used. The two-dimensional electron gas of the 50-nm technology is confined in an $In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ composite channel, whereas the 35-nm technology uses a pure $In_{0.8}Ga_{0.2}As$ channel. The T-gates are defined by electron beam lithography and are encapsulated in BCB. The wafer is passivated with a 250-nm-thick SiN layer, which also acts as the dielectric layer of the on-wafer MIM capacitors and is deposited by CVD. Further passive elements comprise NiCr thin-film resistors, an electron beam evaporated Au based interconnection layer, and a 2.7-µm-thick plated Au layer in air-bridge technology. The 35-nm technology features a second evaporated Au interconnection layer between the first and the galvanic metallization. The first and the second interconnection layer are separated by a second BCB layer with a thickness of 1.4 µm. After finishing the front-side process, a full back-side process follows. This includes wafer thinning to 50-µm thickness, through substrate via-holes, and back- side metallization. Table I summarizes the key performance parameter of the two mHEMT technologies.

Table I: Key Parameters of the mHEMT Technologies

	50-nm mHEMT	35-nm mHEMT
Electron Mobility ($cm^2/(V*s)$)	11800	9800
Electron Density ($1/cm^2$)	$4.2*10^{12}$	$6.1*10^{12}$
Max. Drain Current (mA/mm)	1300	1600
Breakdown Voltage (V)	3.0	2.0
Max. Transconductance (mS/mm)	2100	2500
Transition Frequency (GHz)	380	515
Max. Oscillation Frequency (GHz)	≈ 670	> 1000

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3 Evaluation of the Cryogenic Performance of the 35-nm and 50-nm mHEMT Technologies

The investigation of the noise performance of the two mHEMT technologies is done on bases of two W-band LNA MMICs. First, we describe the design of the MMIC und the room-temperature performance measured on wafer. Afterwards, we analyze the cryogenic performance based on two waveguide modules.

3.1 Low-Noise Amplifier MMIC Design

For maximum comparability of the two utilized mHEMT technologies, the topology of the two LNAs is identical and the entire MMIC design was kept as similar as possible. The LNAs comprise four stages, with a common-source (CS) transistor per stage. A simplified schematic of an amplifier stage is depicted in Figure 1. The design targets for the LNAs are an operating frequency bandwidth which covers at least the extended W-band, with a gain of more than 20 dB, and the lowest achievable noise figure for the entire bandwidth. The amplifiers are designed in a grounded coplanar waveguide environment. Chip photographs of the designed and fabricated LNA MMICs are shown in Figure 2. Including the RF and DC pads, the occupied chip area for each MMIC is 1.5

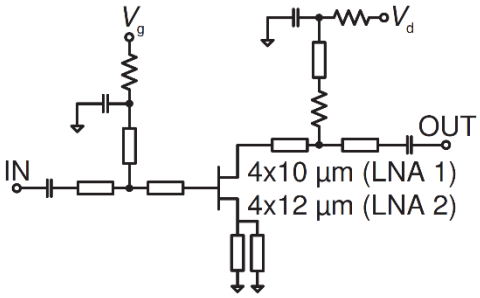

Figure 1: Simplified schematic of an amplifier stage.

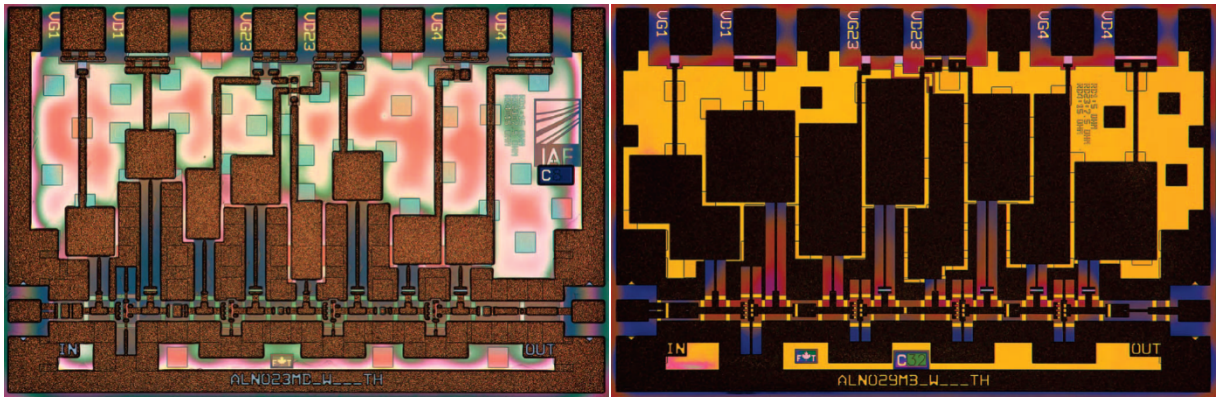

Figure 2: Chip photographs of the presented LNA MMICs, (left) LNA1: 35-nm mHEMT and (right) LNA2: 50-nm mHEMT technology. The dimensions of both chips are 1.5 mm x 1 mm.

mm x 1 mm.

In order to achieve a wideband performance, especially regarding the noise figure, three design issues are most important: inductive source degeneration in all stages, the optimum transistor gate width (W_g), and wideband RF-shorted stubs at gate and drain of the HEMTs. Inductive source degeneration is a common technique for the first stage of an LNA to achieve simultaneous input noise and power matching. The quality factor (Q) of the series RLC resonator of the transistor input is $Q \propto C_{gs}/L_s$, where C_{gs} is the gate-source capacitance of the transistor. L_s is the inductance (due to the source line) which is provided to the source of the transistor. From this equation, it can be seen that increasing L_s reduces Q and makes an improved wideband matching feasible. Hence, source degeneration is used for all stages. The length of the source line for the stages two to four

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of LNA2 is 30 µm. Since LNA1 uses transistors with an asymmetric source-line configuration for these stages, the length of the source-line is halved (15 µm).

For an optimum W_g, different criteria have to be fulfilled. Firstly, it is necessary that, especially for the first stage of an LNA, a simultaneous input noise and power matching is easily achieved with less passive components in front of the first transistor. Secondly, the inductive source degeneration of the first stage should be as small as possible because it decreases the gain of a transistor. Thirdly, since the noise figure increases with longer transistor fingers, each finger should be as short as possible. To find a trade-off, several correlations can be observed from simulations. To fulfill the first criterion, W_g should be about 60 µm for both technologies. On the one hand, relatively long transistor fingers disagree with the third criterion. On the other hand, short transistor fingers require a relatively large source degeneration, which disagrees with the second criterion. In

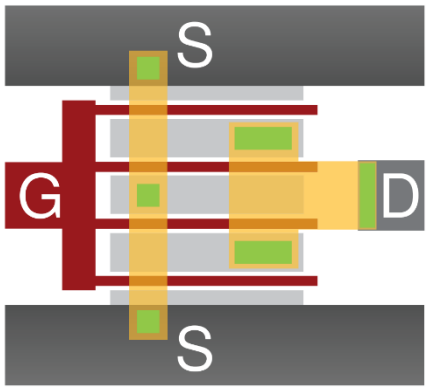

Figure 3: Simplified layout of a CS transistor including the novel drain feeder.

addition, very short transistor fingers show a distinct drop in RF performance due to parasitic effects. Thus, the trade-off for W_g of LNA1 and LNA2 is 40 µm and 48 µm, respectively. The corresponding length of the symmetrical source lines is 60 µm for the first stage of both LNAs. To satisfy the third criterion, transistors with four fingers are used. Thus, the gate width configuration for the transistors of LNA1 and LNA2 is 4x10 µm and 4x12 µm, respectively.

A third possibility to further improve the wideband performance of an amplifier is to use RF-shorted stubs with a high characteristic impedance. The higher the impedance of the transmission line (TL) is the shorter a stub can be, in order to present the same impedance to the circuit. Thus, the equivalent inductance of a shorted stub gets more independent of the operating frequency. Consequently, all RF-shorted stubs and source lines utilize TLs with a width and a characteristic impedance of 4.5 µm and 83 Ω, respectively. It was observed by [1] and [7] that high-speed transistor technologies are prone, especially for cryogenic conditions, to oscillations inside a transistor, which uses more than two transistor fingers. Thus, a new optimized drain feeder was designed (as exemplified in Figure 3), which connects the two drain areas of a four finger transistor and the transmission line at the output of the transistor via an air-bridge with three posts. Thereby, due to a decreased effective electrical length between the two drain areas, we demonstrated in [7] that the tendency of odd-mode oscillations inside a transistor is reduced. Furthermore, the new drain feeder improves the wideband performance of the LNAs, since the series inductance, by which the stub is connected to the drain of each transistor, is reduced. In order to guarantee unconditional stability, all stages (except of the first stage of LNA2) contain a 10-Ω resistor at the beginning of the drain stubs. The gate stub of the last stage of each LNA includes a 10-Ω resistor as well.

3.2 Room-Temperature On-Wafer Measurements

The S-parameters of the two LNA MMICs were measured using an on-wafer probe station with an Anritsu VectorStar system. In Figure 4, the measured S-parameters are given for noise-optimized biasing conditions for a frequency range from 0 to 140 GHz. The corresponding drain voltage and drain current density of LNA1 (35-nm mHEMT) and LNA2 (50-nm mHEMT) are V_d = 0.8 V and j_d = 300 mA/mm and V_d = 0.6 V and j_d = 250 mA/mm, respectively. LNA2 yields a gain of more than

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20 dB for frequencies between 49-117 GHz, with a peak gain of 27 dB between 57-72 GHz. LNA1 exhibits a gain of more than 23 dB for a frequency range from 52 to 126 GHz, with a peak gain of 28 dB between 57-76 GHz. The measured and simulated S-parameters of LNA2 match very well.

The noise figure of the LNA MMICs was measured on-wafer for W-band frequencies from 75 to 110 GHz. The measured noise figure of LNA1 and LNA2 is depicted in Figure 4 versus frequency for the entire W-band. LNA2 achieves a noise figure between 1.8-2.6 dB, with an average value of 2.1 dB. LNA1 exhibits a noise figure between 1.6-2.2 dB, with an average value of 1.9 dB. Both MMICs show an excellent agreement between measured and simulated noise figures. Moreover, the noise figure of both LNAs was measured for a wide range of biasing conditions. A contour plot is given in Figure 4. For each supporting point (black circles) the noise figure is averaged over the entire W-band. The comparison of the contour plot of both LNAs exhibits an excellent noise performance, with less than an average noise figure of 2.5 dB, over a wide range of biasing conditions. However, LNA1 provides even more flexibility in biasing and still provides, for instance, an average noise figure of less than 2.1 dB for an output power optimized bias point, with a supply voltage of 1 V.

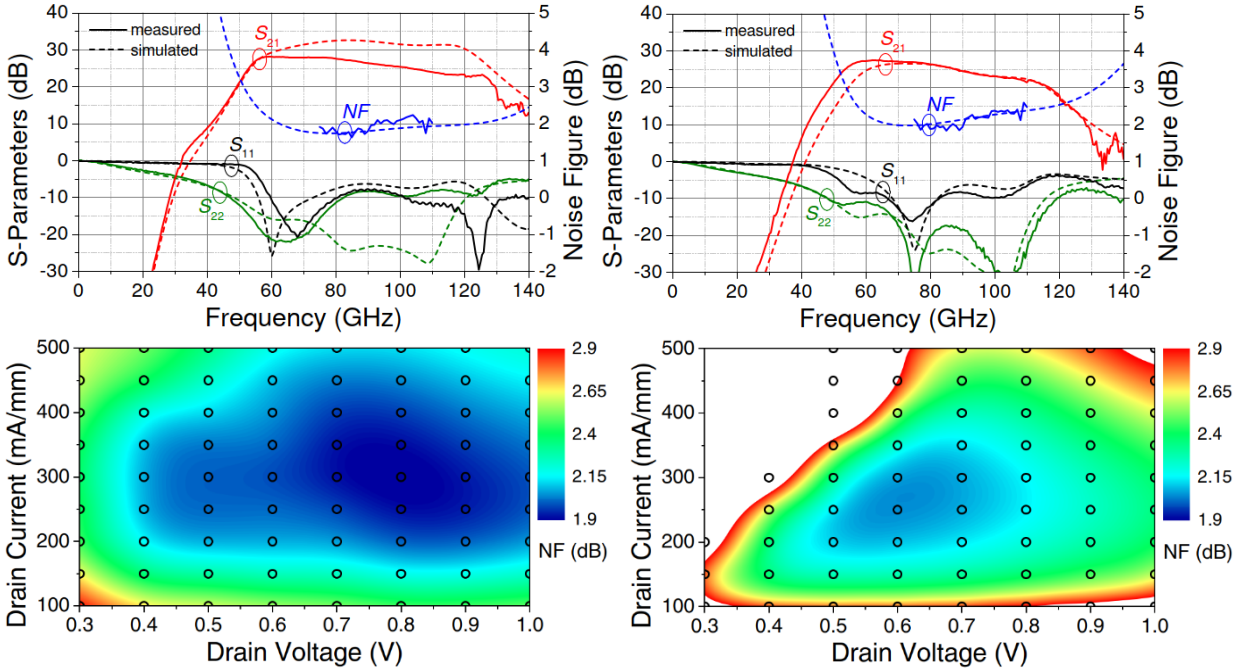

Figure 4: (Top) Measured (solid lines) and simulated (dashed lines) S-parameters and noise figure of the presented LNA MMICs. S-parameters and noise figure are given for noise-optimized biasing conditions: (Left: LNA1) V_d = 0.8 V and j_d =300 mA/mm and (right: LNA2) V_d = 0.6 V and j_d = 250 mA/mm. (Bottom) Contour plot of the measured noise figure versus drain voltage and drain current density of the presented LNAs. The noise figure was measured for the given supporting points (black circles) and is averaged over the entire W-band (75-110 GHz). White areas exhibit a noise figure of more than 2.9 dB.

3.3 Module Measurements

The MMICs are packaged in WM-2540 (formerly WR-10) waveguide gold-plated brass modules. E-plane transitions are used at the input and output of the MMICs for a connection to the waveguide. The E-plane transitions are fabricated on 50-µm-thick quartz substrates. An interior view of an assembled LNA module, including DC and RF wire bonds, is given in Figure 5.

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3.3.1 Room-Temperature Module Measurements

The room-temperature measurement results are depicted in Figure 6 for noise-optimized biasing conditions. LNA2 is biased with a drain voltage (V_d; on transistor level) and a drain current (j_d) of 0.7 V and 250 mA/mm, respectively. This results in a total power consumption of the module of 36.3 mW. The S-parameters are measured from 67 to 115 GHz (limits of the S-parameter setup) and yield an average small-signal gain of 22.2 dB (19.5 to 24.7 dB). In the frequency range from 70 to 116 GHz (limits of the noise setup), the noise temperature is 196 to 291 K with an average of 247 K. This results in a noise figure of 2.2 to 3 dB (average: 2.6 dB).

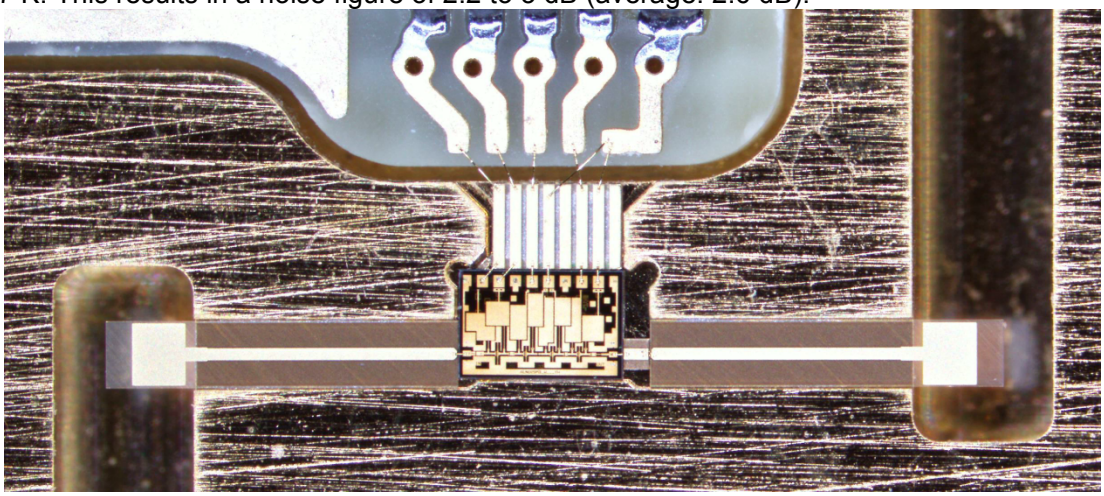

Figure 5: Close-up view of an assembled WM-2540 waveguide LNA module with a 50-nm gate-length MMIC (LNA2). LNA1 is assembled similarly.

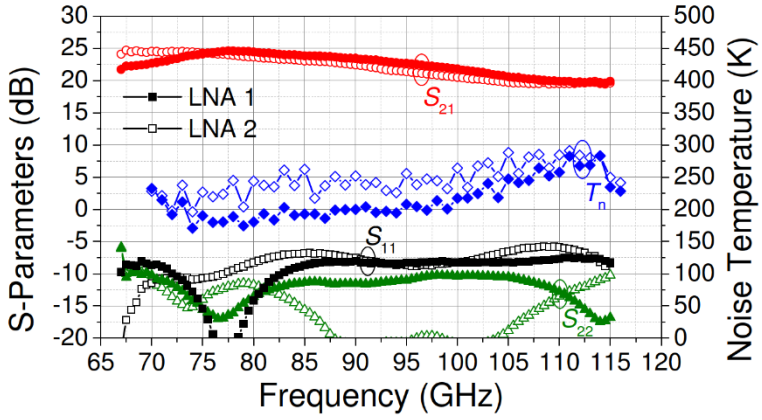

Figure 6: Measured S-parameters and noise temperature of the presented LNA1 (filled symbols) and LNA2 (blank symbols) at room temperature. S-parameters and noise temperature are given for noise-optimized biasing conditions (on transistor level). LNA1: V_d = 0.6 V and j_d = 250 mA/mm (first stage) and V_d = 0.8 V and j_d = 250 mA/mm (second to fourth stage). LNA2: V_d = 0.7 V and j_d = 250 mA/mm.

LNA1 is biased (on transistor level) with V_d = 0.6 V and j_d = 250 mA/mm (first stage). The other stages are biased with a V_d and j_d of 0.8 V and 250 mA/mm, respectively. Hence, the total power consumption of the module is 58.6 mW. LNA1 achieves an average small-signal gain of 22.6 dB (19.6 to 24.6 dB). The noise temperature is between 171 to 283 K with an average of 214 K. The resulting noise figure is 2 to 2.9 dB (average: 2.4 dB). Assisted by Monte Carlo analysis, the measured noise temperature of the amplifiers includes an uncertainty of about ±25 K (2σ).

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3.3.2 Cryogenic Module Measurements

At cryogenic temperatures, the noise measurement were done at Yebes Observatory. The setup is based on the Y-factor method with a heated load. The hot and cold states are 50 and 20 K, respectively. The mixer at the output of the DUT for the down conversion of the test signal is outside the cryostat at room temperature. The measured noise performance is corrected for the contribution of the down-converter noise, but includes the losses of the waveguide at the output of the DUT and the vacuum window. Thus, the measured gain is slightly lower than the actual gain of the LNAs. The measurements are performed over the entire 70-116-GHz frequency range.

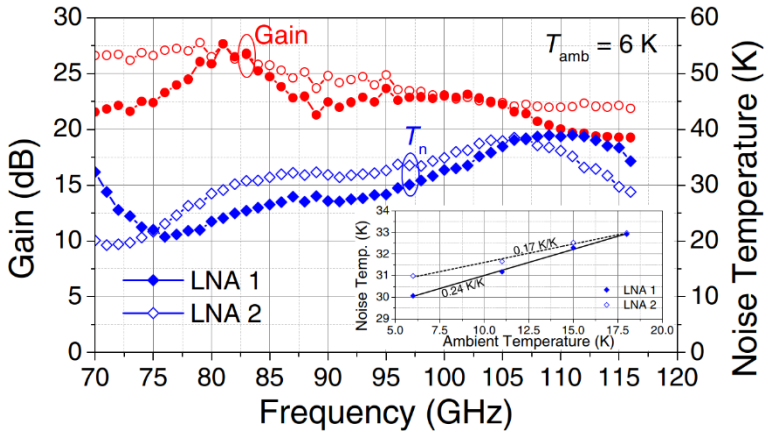

Figure 7: Measured noise temperature and gain of the presented LNA1 (filled symbols) and LNA2 (blank symbols) at an ambient temperature of 6 K. The results are given for noise-optimized biasing conditions (on transistor level). LNA1: V_d = 0.5 V and j_d = 137.5 mA/mm and LNA2: V_d = 0.4 V and j_d = 146 mA/mm (first stage) and V_d = 0.7 V and j_d = 146 mA/mm (second to fourth stage). Additionally, the average noise temperature is given for ambient temperatures from 6 to 18 K.

In Figure 7, the measured noise temperature and gain versus operating frequency are depicted at an ambient temperature of 6 K for noise-optimized biasing conditions. Additionally, Figure 7 shows the average noise temperature for ambient temperatures of 6, 11, 15, and 18 K for the same values of V_d and j_d. In the first stage, LNA2 is biased with a V_d and j_d of 0.4 V (on transistor level) and 146 mA/mm, respectively. The other stages are biased with the same j_d, whereas V_d is 0.7 V. The total power consumption of the LNA module is 28.8 mW. For an ambient temperature of 15 K, the obtained average noise temperature is 32.5 K (20.6 to 40.1 K) with a minimum noise temperature of 20.6 K at 71 GHz. The corresponding gain is between 21.8 and 27.7 dB with an average of 24.8 dB. When cooling down to an ambient temperature of 6 K, the measured noise temperature is reduced to an average value of 31 K (19.2 to 38.5 K) with a minimum noise temperature of 19.2 K at 71 GHz. For the measurements versus ambient temperature, LNA2 exhibits a linear slope (noise temperature per ambient temperature) of 0.17 K/K, whereas the gain remains almost constant.

LNA1 is biased, in all stages similarly, with a V_d (on transistor level) and j_d of 0.5 V and 137.5 mA/mm, respectively. The total power consumption of the LNA module is 17 mW. For an ambient temperature of 15 K, the achieved average noise temperature is 32.2 K (23.0 to 41.9 K) with a minimum noise temperature of 23 K at 76 GHz. The corresponding gain is between 19.1 and 28.0 dB with an average of 23.1 dB. When cooling down to an ambient temperature of 6 K, the measured noise temperature is reduced to an average value of 30.1 K (20.7 to 39.0 K) with a minimum noise temperature of 20.7 K at 76 GHz. LNA1 yields a linear slope of 0.24 K/K when varying the ambient temperature from 6 to 18 K. As for LNA2, the gain of LNA1 stays almost constant. The measured cryogenic noise temperature of the amplifiers includes an uncertainty of about ±1.4 K (2σ).

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For a comprehensive comparison of the utilized mHEMT technologies, gain and noise of the two LNAs are measured for various biasing conditions. In Figure 8, contours of the obtained noise temperature and gain are given for an ambient temperature of 15 K. Black circles indicate measurements over the 70-116-GHz frequency range. The gain of the LNAs versus bias behaves very similarly. As already illustrated in Figure 7, the average noise temperature for an optimized bias is almost identical. LNA2 tolerates a wide area of biasing conditions. However, the noise contour of LNA1 indicates that the 35-nm gate-length mHEMT technology is slightly more flexible in biasing the amplifier. For instance, V_d can be varied from 0.25 to 0.8 V and a wide range of drain currents with still an average noise temperature of less than 36 K.

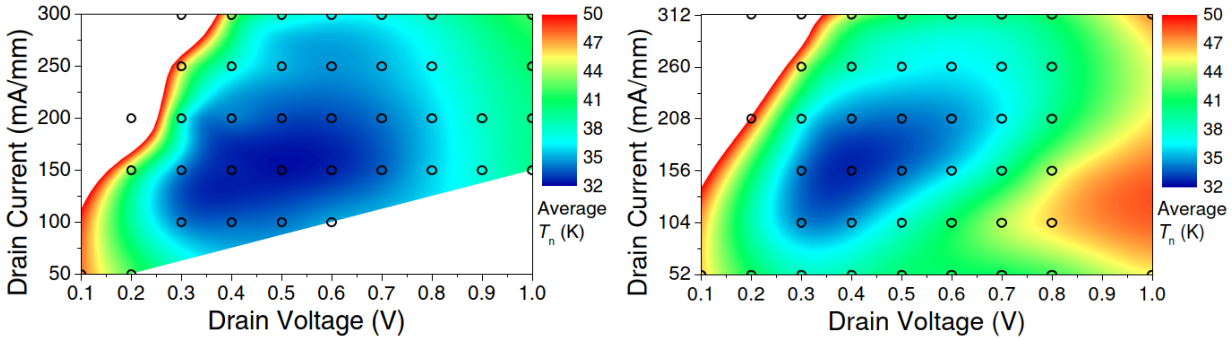

Figure 8: Contour plots of the measured noise temperatures versus V_d and j_d of the first stage of the LNAs at an ambient temperature of 15 K. The bias of the other stages is kept constant. The noise temperatures are measured for the given supporting points (black circles) and are averaged over the entire frequency range from 70 to 116 GHz. White areas exhibit noise temperatures of more than 50 K.

3.4 Discussion

The comparison of the achieved room-temperature and cryogenic performance of LNA1 and LNA2 exhibits an improvement of the average noise temperatures, when cooling the amplifiers, by a factor of 7.1 and 8, respectively. It can be observed that, at lower frequencies, the cryogenic noise temperature of both LNAs improves more than at higher frequencies.

Both LNAs exhibit an excellent gain and noise performance at room temperature and cryogenic conditions. At room temperature, LNA1 and LNA2 obtain an average gain of 22.6 and 22.2 dB and an average noise temperature of 214 and 247 K (noise figure: 2.4 and 2.6 dB), respectively. The lowest-achieved noise temperatures are 171 and 196 K (noise figure: 2 and 2.2 dB). The presented LNAs obtain the lowest average noise temperatures at room temperature over the 70-116-GHz band. Simultaneously, LNA1 and LNA2 yield average cryogenic noise temperatures of 30.1 and 31 K with a minimum value of 20.7 and 19.2 K at 76 and 71 GHz, respectively. Thus, the achieved cryogenic noise performance of the LNAs is among the best noise temperatures published so far. Furthermore, the results demonstrate that mHEMT and InP HEMT technologies achieve comparable noise performances.

4 New Noise-Improved 50-nm mHEMT Technology

The observations that the measured noise temperature (at room temperature as well as cryogenic conditions) of the 35-nm mHEMT technology depends less on the applied bias than for the standard 50-nm mHEMT technology is an important results of the first experiment, which is described in Section 3. In general, one would consider a stronger bias dependence of RF characteristics as a short-channel effect. However, in the comparison between the two technologies, the standard 50-nm mHEMT technology shows a stronger dependence. These results were the initiator for a further investigation on how the existing standard 50-nm mHEMT technology can be improved so that these short-channel effects are optimized. This could potentially improve the noise performance, especially at cryogenic conditions, so that this

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optimized 50-nm technology would provide an improved noise performance even compared to the 35-nm mHEMT technology.

4.1 Description of the Noise-Improved 50-nm mHEMT Technology

The investigation of the new noise-improved 50-nm mHEMT technology is based on the hypotheses that the composite channel, which is used in the standard 50-nm technology but not in

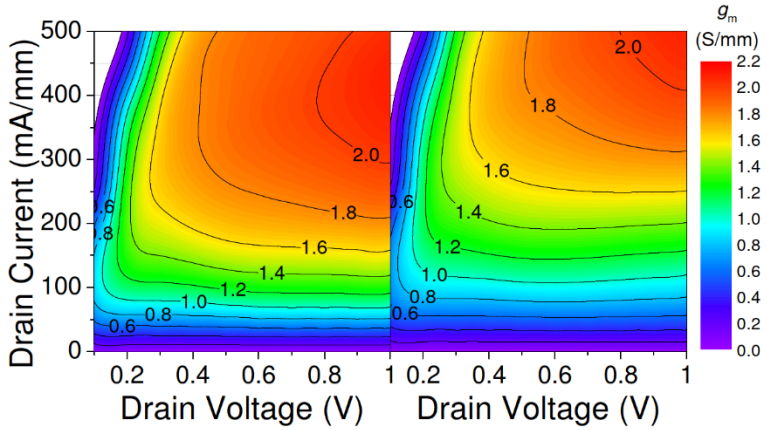

Figure 9: Contour plots of the measured DC transconductance of (left) the new 50-nm mHEMT and (right) the standard 50-nm mHEMT technology. Drain voltage and current of a 2 x 60 µm transistor are varied from 0.1 to 1 V and 50 to 500 mA/mm, respectively.

the 35-nm mHEMT technology, is mainly responsible for the stronger bias dependence of the 50-nm mHEMT technology. Thus, we developed a new 50-nm mHEMT technology with the intention to improve the noise performance in general but especially for cryogenic operation. Therefore, we omitted the sub-channel of the composite channel so that a single $In_{0.8}Ga_{0.2}As$ channel is used (as it is also the case in the 35-nm mHEMT technology).

In Figure 9, the dc g_m of 2 x 60 µm transistors that are fabricated in the new 50-nm mHEMT (left) and the standard 50-nm mHEMT technology (right) is shown. The drain voltage (V_d) and current (I_d) at the device level are varied from 0.1 to 1 V and 50 to 500 mA/mm, respectively. For both technology versions, the maximum g_m is about 2100 mS/mm. However, while the standard technology requires a drain current of more than 500 mA/mm, achieves the new technology peak g_m for less than 400 mA/mm. Furthermore for noise-optimal drain currents (75 to 200 mA/mm), the transconductance of the new technology is about 300 mS/mm higher than for the standard technology; e.g. at a bias of V_d = 0.6 V and I_d = 200 mA/mm, g_m reaches for the new and standard technology 1.71 and 1.44 mS/mm, respectively. Thus, already the given DC data indicate that the new 50-nm mHEMT technology offers advantages at common low-noise bias conditions. Both technologies feature typical drain-gate breakdown voltages of >3 V (@ I_g = 1 mA/mm).

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4.2 Room-Temperature On-Wafer Measurements

At room temperature, the RF performance, especially the noise temperature, is again verified by using measurements of a W-band LNA MMIC, which is similar to the MMIC that is explained in Section 3. In Figure 10, the S-parameters and noise temperature of the LNA MMIC fabricated in the new 50 nm mHEMT technology are depicted. The circuit is biased for optimum noise

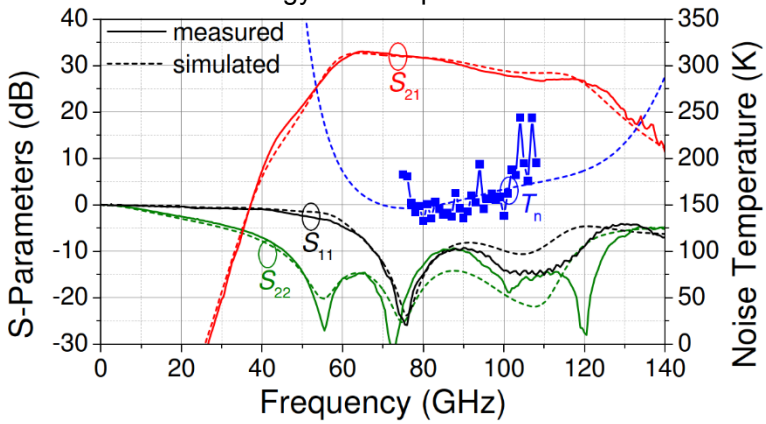

Figure 10: Measured and simulated (dashed lines) on-wafer S-parameters and noise temperature versus operating frequency of the LNA MMIC fabricated in the new 50-nm mHEMT technology. The LNA is biased for optimum noise with a drain voltage at transistor level of 0.6 V and a drain current of 200 mA/mm.

performance with a drain voltage and current of 0.6 V and 200 mA/mm. The LNA yields a small-signal gain of more than 25 dB over a frequency range from 60 to 124 GHz. At 65 GHz, a peak gain of 33 dB is achieved. The input and output return loss is better than 10 dB over most part of the band. The noise temperature exhibits an average value of 159 K (NF = 1.9 dB) with values between 132 and 243 K (1.6 to 2.6 dB). The simulations are illustrated as dashed line in Figure 10 and a very good agreement with the experiment can be observed.

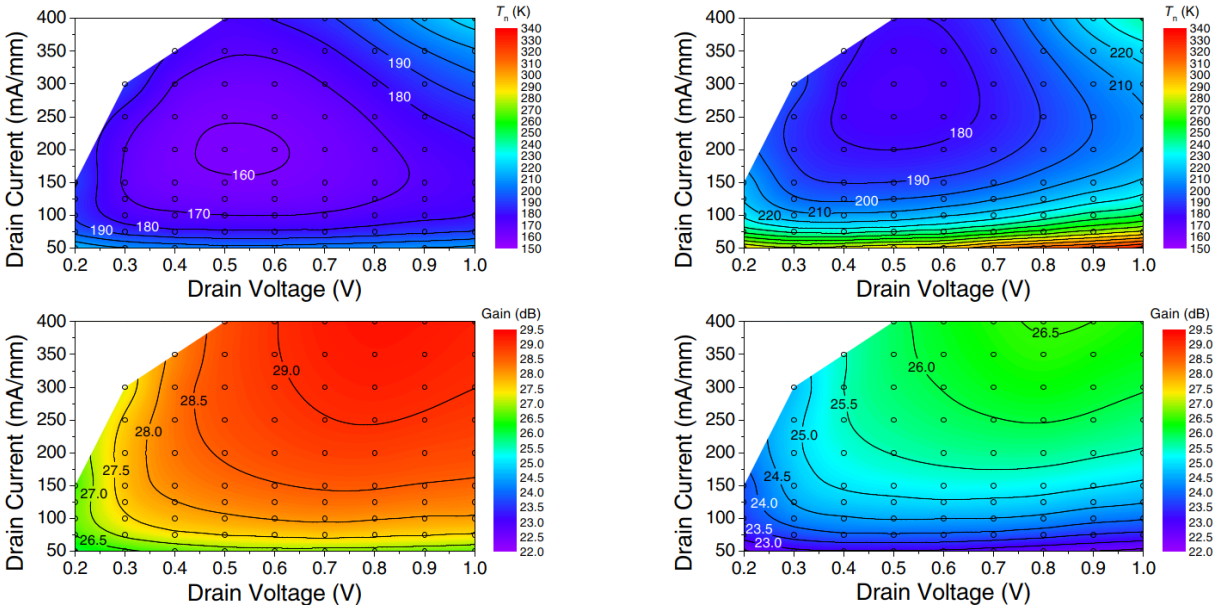

Figure 11: Contour plots of the on-wafer measured T_n and gain versus V_d and I_d of the first stage of the LNA. Left and right show the measured data for the new and standard 50 nm mHEMT technology. The bias of the other stages is kept constant. Gain and T_n are measured for the given supporting points (black circles) and are averaged over the entire frequency range from 75 to 108 GHz.

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The measured results for investigating the bias dependence of the technologies are illustrated in Figure 11. For this experiment, the bias only of the first stage was varied between V_d = 0.2 - 1 V and I_d = 50 - 400 mA/mm. Low drain voltages and high drain currents were excluded in order to prevent the gate diode to get conductive. The bias of the latter stages is fixed at V_d = 0.6 V and I_d = 200 mA/mm for the new 50-nm mHEMT technology and V_d = 0.6 V and I_d = 250 mA/mm for the standard 50-nm mHEMT technology. For each supporting point, a noise and gain measurement were performed and averaged. The gain contours of both technologies are comparable with a slightly higher gradient for currents below 100 mA/mm for the standard 50-nm mHEMT technology. However, a more obvious difference between the new and the standard 50-nm mHEMT technology is a gain difference of about 3 dB. The benefit of the new 50-nm mHEMT technology is even more distinct when considering the noise contour. First of all, the new 50-nm mHEMT technology has a noise advantage of 15 K at the noise-optimal bias point which is at a drain current of 200 mA/mm, whereas the standard 50-nm mHEMT technology requires a drain current of 300 mA/mm for optimum noise performance. Furthermore, the contour of the new 50-nm mHEMT technology is much more flat. While the new 50-nm mHEMT technology achieves a noise temperature of 180 K (2.1 dB), which is only an increase of about 20 K, over a large bias range, a comparable area for the standard 50 nm mHEMT technology is much smaller. In addition, the noise temperature degrades stronger for drain currents below 100 mA/mm.

4.3 Cryogenic Noise-Temperature Measurements

Based on the very promising results of the on-wafer measurements at room temperature, the new 50-nm mHEMT technology is tested at cryogenic temperatures on module level. The assembly of the test modules and the cryogenic noise measurements were done at the Max Planck Institute for Radio Astronomy. The setup is based on the Y-factor method. For the measurements, the LNA

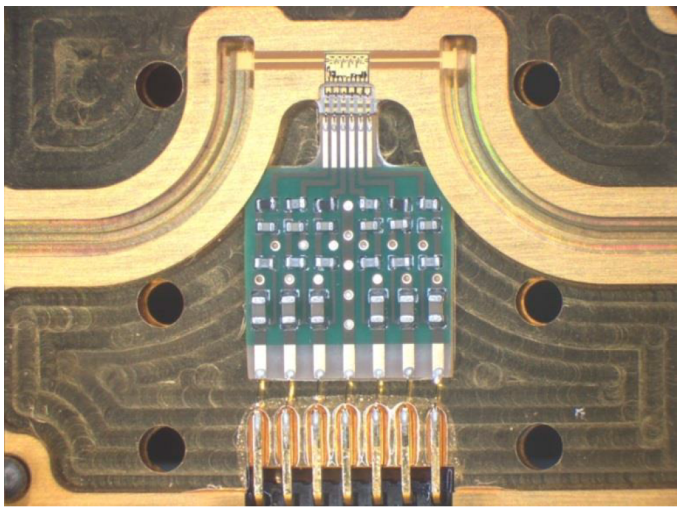

Figure 12: Close-up view of an assembled WM-2540 waveguide LNA module with the new 50-nm mHEMT technology for noise testing at cryogenic conditions.

module is mounted in a vacuum chamber with a Mylar window. With a waveguide horn at the input of the LNA, temperature loads at liquid nitrogen (77 K) and room temperature are presented to the LNA. The downconverter module is outside the cryostat at room temperature.

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Figure 12 shows a close-up view of an assembled waveguide module. The measured performance for different bias conditions is illustrated in Figure 13. For a frequency range from 66-116 GHz and a bias current of 100 mA/mm, the measured average noise temperature is 29.1 K. It is important to mention that the losses of the vacuum window and the waveguide horn in front of the LNA are part of the measured performance. Since the measurement setup in Section 3.3.2 uses a heated load, only the LNA module determines the measured noise temperature in Section 3.3.2. Thus, it can be concluded that the measured noise temperature in this section should be understood as conservative and might give even lower noise temperatures when measured in the setup of Section 3.3.2.

The measured noise temperature proofs that the new 50-nm mHEMT technology improves the noise performance at room temperature and cryogenic conditions when compared to the previously existing standard 50-nm mHEMT technology as well as the 35-nm mHEMT technology.

5 Conclusions

Three major achievements can be concluded of the described work in WP5.1.1 of RadioNet. The first important results is that we are able to demonstrate that mHEMT and InP HEMT technologies can obtain comparable noise temperatures at cryogenic conditions, which was not demonstrated before. This is already a result of the first experiment where we compared the existing Fraunhofer IAF standard 50-nm and 35-nm mHEMT technologies. The second achievement is that both technologies exhibit a comparable noise performance at cryogenic temperatures. Thus, it can be concluded that the 35-nm mHEMT technology offers no major benefit but also no drawback for a cryogenic operation when compared to the standard 50-nm mHEMT technology. At room temperature, a slight advantage of the 35-nm mHEMT technology over the 50-nm mHEMT technology can be observed. The third and final achievement is that based on the first experiment, a noise-improved new 50-nm mHEMT technology was developed. This technology outperforms the

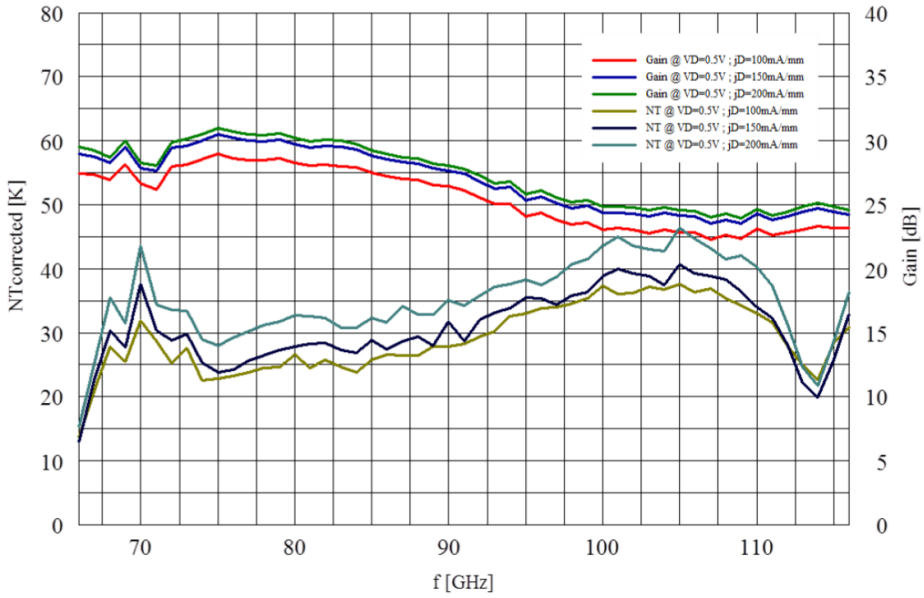

Figure 13: Measured noise temperature and gain at an ambient temperature of 13 K versus operating frequency for different bias conditions.

standard 50-nm mHEMT and 35-nm mHEMT technology at cryogenic temperatures and achieve the same performance as the 35-nm mHEMT technology at room temperature. This is a very valuable results for the work in RadioNet and beyond.

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6 Acronyms

BCB	Benzocyclobutene
CVD	Chemical vapor deposition
IAF	Fraunhofer Institute for Applied Solid State Physics IAF
InP	Indium phosphide
LNA	Low-noise amplifier
mHEMT	Metamorphic high-electron-mobility transistor
MIM	Metal-insulator-metal
MMIC	Monolithic microwave integrated circuit
MPIfR	Max Planck Institute for Radio Astronomy
NiCr	Nickel chromium
SiN	Silicon nitride

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